



KINGSTON ENGINEERING COLLEGE

(An Autonomous Institution)

**(Approved by AICTE & COA, New Delhi, Affiliated to Anna University, Chennai)
Chittoor Main Road, Christianpet,
Katpadi, Vellore-632059**

MASTER OF ENGINEERING IN APPLIED ELECTRONICS

AUTONOMOUS CURRICULUM

REGULATION 2026

Academic Year 2026-27 onwards



INSTITUTE VISION

To be a pioneer in engineering and management education by providing amicable ambience and being a centre for learning thereby perpetuating versatile professionals in engineering and management suitable for industry, higher education and research.

INSTITUTE MISSION

- Developing, nurturing and building professionals with technical, research and managerial expertise, intellectual proficiency, right attitude and moral ethics.
- Building infrastructure that earmarks the institution to be the most preferred educational destination and provides the right ambience for creative and innovative teaching - learning process.
- Enabling learners to broaden their horizon and helping to meet global challenges.

QUALITY POLICY

To establish and implement a robust quality system at Kingston Engineering College, encircling teaching, learning, research, and self-reliance, focusing on core and support functions to ensure accountability to stakeholders through continuous improvement and sustenance towards promoting holistic academic excellence.

TABLE OF CONTENTS

S. NO	DESCRIPTION	PAGE NUMBER
1	Department Vision and Mission	1
2	Program Educational Objectives (PEOs)	1
3	Program Outcomes (POs)	1
4	Program Specific Outcomes (PSOs)	2
5	Mapping of PEOs with POs	2
6	Mapping of PEOs with PSOs	2
7	Curriculum for Semester I to IV	3
8	Credit Distribution	5
9	Programme Elective Courses	6



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. – APPLIED ELECTRONICS

REGULATION – 2026

CHOICE BASED CREDIT SYSTEM

VISION

To develop the department into a Centre of Excellence for learning in the recent trends of Electronics and Communication Engineering, thereby enabling our graduates to excel as efficient engineers, managers, and entrepreneurs.

MISSION

M1: Providing quality education in the areas of Electronics and Communication Engineering to enhance the employability and professional competence of our graduates and contribute to economic, scientific, and societal development.

M2: Endowing students with the knowledge, technical skills and values that prepare them to excel as engineers and leaders in their profession and to be committed to lifelong learning.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

- To enable graduates to develop solutions to real world problems in the frontier areas of Applied Electronics.
- To enable the graduates to adapt to the latest trends in technology through self-learning and to pursue research to meet out the demands in industries and Academia.
- To enable the graduates to exhibit leadership skills and enhance their abilities through lifelong learning.
- To become entrepreneurs to develop indigenous solutions.

PROGRAM OUTCOMES (POs)

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Ability to design and implement innovative solutions to solve complex problems in Applied Electronics.

PSO2: Competence to independently undertake research projects involving simulation, measurement, and product development in Applied Electronics-related fields.

MAPPING OF PROGRAM EDUCATIONAL OBJECTIVES WITH PROGRAM OUTCOMES

PEOs / POs	PO1	PO2	PO3
PEO1	3	2	3
PEO2	3	2	3
PEO3	2	3	2
PEO4	3	2	3

MAPPING OF PROGRAM SPECIFIC OUTCOMES WITH PROGRAM OUTCOMES

PSOs / POs	PO1	PO2	PO3
PSO1	3	2	3
PSO2	3	3	3

SUSTAINABLE DEVELOPMENT GOALS (SDG)



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. – APPLIED ELECTRONICS

REGULATION – 2026

CURRICULUM SEMESTER I to IV

CHOICE BASED CREDIT SYSTEM

(For the Students admitted from the Academic Year 2026-27)

Semester I									
S. No	Course Code	Course Name	Course Type	Contact Periods	L	T	P	C	SDG
Theory Course									
1	AE26M01	Applied Mathematics for Electronics Engineers	BS	4	3	1	0	4	4, 9
2	AE26101	Material Science for Electronics Engineers	PC	3	3	0	0	3	4, 9
3	AE26102	Sensors, Actuators and Interface Electronics	PC	3	3	0	0	3	9, 11
4	AE26103	Advanced Digital System Design	PC	3	3	0	0	3	9, 12
Lab Integrated Theory Course									
5	AE26104	IOT System Design and Security	PC	5	3	0	2	4	9, 7
6	AE26105	Statistical Signal Processing and Modeling	PC	4	2	0	2	3	9, 3
Practical Course									
7	AE26111	Electronic System Design Laboratory	PC	4	0	0	4	2	4, 9
TOTAL				26	17	1	8	22	-

Semester II									
S. No	Course Code	Course Name	Course Type	Contact Periods	L	T	P	C	SDG
Theory Course									
1	AE26201	Digital CMOS VLSI Design	PC	3	3	0	0	3	9, 7
2		Programme Elective I	PE	3	3	0	0	3	-
3		Programme Elective II	PE	3	3	0	0	3	-
4		Programme Elective III	PE	3	3	0	0	3	-
Lab Integrated Theory Course									
5	AE26202	Embedded System Design	PC	5	3	0	2	4	11, 9
Practical Course									
6	AE26211	Analog and Digital CMOS VLSI Design Laboratory	PC	4	0	0	4	2	9, 4
Employability Enhancement Course									
7	AE26S01	Industry Oriented Course	EE	1	1	0	0	1	-
8	AE26S02	Technical Seminar and Research Communication	EE	2	0	0	2	1	4, 9, 17
Mandatory Course									
9	AE26S03	Self-Learning Course	SL	-	-	-	-	0	-
TOTAL				24	16	0	8	20	-

Semester III									
S. No	Course Code	Course Name	Course Type	Contact Periods	L	T	P	C	SDG
Theory Course									
1		Programme Elective IV	PE	3	3	0	0	3	-
2		Programme Elective V	PE	3	3	0	0	3	-
Lab Integrated Theory Course									
3	AE26301	Digital Image and Video Processing	PC	5	3	0	2	4	9, 3
Practical Course									
6	AE26311	Project Work – I	EE	12	0	0	12	6	-
TOTAL				23	9	0	14	16	-

Semester IV									
S. No	Course Code	Course Name	Course Type	Contact Periods	L	T	P	C	SDG
1	AE26411	Project Work – II	EE	24	0	0	24	12	-
TOTAL				24	0	0	24	12	-

Credit Distribution

S.No.	Subject Area	Credit Per Semester				Credits Total	Percentage
	Semester	I	II	III	IV		
1	Basic Science (BS)	4	0	0	0	4	5.7 %
2	Employability Enhancement (EE)	0	2	6	12	20	28.6 %
3	Professional Course (PC)	18	9	4	0	31	44.3 %
4	Programme Elective (PE)	0	9	6	0	15	21.4 %
5	Mandatory Course	-	-	0	-	0	0
Total		22	20	16	12	70	100

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. – APPLIED ELECTRONICS

PROGRAMME ELECTIVE COURSES

S. No	Course Code	Course Name	Course Type	Contact Periods	L	T	P	C	SDG
1	AE26001	Nano Electronics and Technology	PE	3	3	0	0	3	9, 3, 7, 13
2	AE26002	Cyber Security for Electronics System	PE	3	3	0	0	3	9, 4, 8
3	AE26003	RF Integrated Circuit Design	PE	3	3	0	0	3	9, 7
4	AE26004	Electromagnetic Interference and Compatibility	PE	3	3	0	0	3	9, 3, 11
5	AE26005	Advanced Microprocessors and Microcontrollers Architectures	PE	3	3	0	0	3	9, 7, 12
6	AE26006	Advanced Computer Architecture Design	PE	3	3	0	0	3	9, 7, 13
7	AE26007	Signal Integrity for High-Speed Design	PE	3	3	0	0	3	9, 11, 12
8	AE26008	VLSI Interconnects	PE	3	3	0	0	3	9, 7
9	AE26009	Semiconductor Memory Design	PE	3	3	0	0	3	9, 4
10	AE26010	Algorithms For VLSI Physical Design Automation	PE	3	3	0	0	3	9, 8
11	AE26011	Statistical Analysis and Optimization for VLSI	PE	3	3	0	0	3	9, 12
12	AE26012	System on Chip Design	PE	3	3	0	0	3	9, 11
13	AE26013	Hardware /Software Co-Design	PE	3	3	0	0	3	9, 7
14	AE26014	MEMS and NEMS	PE	3	3	0	0	3	9, 3
15	AE26015	Cryptography and Network Security	PE	3	3	0	0	3	16, 9
16	AE26016	Neuromorphic Computing	PE	3	3	0	0	3	9, 7
17	AE26017	AI Hardware Architectures and Accelerators	PE	3	3	0	0	3	9, 4
18	AE26018	IP Core Design and Protection	PE	3	3	0	0	3	9, 8
19	AE26019	Spintronics and Quantum Computing	PE	3	3	0	0	3	9, 7
20	AE26020	Robotics and Intelligent Systems	PE	3	3	0	0	3	9, 11


BOS CHAIRMAN/ECE


PRINCIPAL

SEMESTER I

AE26M01	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS	L	T	P	C
SDG: 4, 9		4	0	0	4
COURSE OBJECTIVES: • Impart the knowledge of Fuzzy set and Fuzzy logic. • Introduce the idea of matrix decomposition. • Implement the fundamental concept of probability. • Acquaint the students with the concepts of dynamic programming. • Develop an understanding on the concepts of queuing theory.					
UNIT I	FUZZY LOGIC	12			
Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.					
UNIT II	MATRIX THEORY	12			
Eigenvectors – Canonical basis – QR factorization – Least squares method – Singular value decomposition.					
UNIT III	PROBABILITY AND RANDOM VARIABLES	12			
Probability – Axioms of probability – Conditional probability – Baye's Theorem – Random variables – Probability function – Moments – Moment generating function.					
ACTIVITIES: Prepare a case study on uncertainty analysis in engineering systems & Review of GATE Questions					
UNIT IV	DYNAMIC PROGRAMMING	12			
Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of Dimensionality.					
UNIT V	QUEUEING MODELS	12			
Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula – Machine interference Model – Steady State analysis – Self-service queue.					
ACTIVITIES: 1. Design fuzzy membership functions for student performance (Poor, Average, Good, Excellent) using any Simulation Tools 2. Implement Fibonacci sequence, shortest path problem, or knapsack problem using recursion and dynamic programming. 3. Simulate M/M/1 and M/M/c queue models using any Simulation Tools. 4. Review of GATE Questions.					
COURSE OUTCOMES: CO1: Apply the concept of fuzzy logic in real-life problems. CO2: Execute the matrix decomposition in engineering problems. CO3: Make use of probability concepts in problems of uncertainty. CO4: Use dynamic programming for optimization. CO5: Analyze and apply the various queuing models.					
TOTAL: 45 PERIODS					
WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%					
TEXTBOOKS: 1. Advanced Engineering Mathematics, Erwin Kreyszig, 10th Edition, John Wiley & Sons, 2023. 2. Fuzzy Sets, Uncertainty and Information, George J. Klir and Tina A. Folger, Prentice Hall, Latest Reprint Edition.					
REFERENCES: 1. Introduction to Probability Models, Sheldon M. Ross, 13th Edition, Academic Press (Elsevier), 2024. 2. Probability and Statistics for Engineers and Scientists, Ronald E. Walpole, Raymond H. Myers, Sharon L. Myers and Keying Ye, 10th Edition, Pearson, 2022. 3. Introduction to Operations Research, Frederick S. Hillier & Gerald J. Lieberman, 11th Edition, McGraw-Hill Education, 2021. 4. Fuzzy Logic with Engineering Applications, Timothy J. Ross, 5th Edition, Wiley, 2023. 5. Introduction to Linear Algebra, Gilbert Strang, 6th Edition, Wellesley-Cambridge Press, 2023.					

6. Fundamentals of Queueing Theory, Donald Gross, John F. Shortle, James M. Thompson and Carl M. Harris, 5th Edition, Wiley, 2018 (Latest Edition).

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	3	2
CO2	2	1	3	3	2
CO3	2	1	3	2	2
CO4	3	1	3	3	3
CO5	2	1	3	2	3
AVG	2.2	1	3	2.6	2.4

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26101	MATERIAL SCIENCE FOR ELECTRONICS ENGINEERS	L	T	P	C
SDG: 4, 9		3	0	0	3
COURSE OBJECTIVES:					
- Understand the structure, properties and characterization of engineering materials used in electronic devices. - Explain the electrical, magnetic, optical and dielectric properties of electronic materials. - Analyze semiconductor materials and fabrication techniques used in modern electronics. - Understand nanomaterials, thin films and advanced functional materials for electronic applications. - Apply material selection concepts for emerging electronic, photonic and energy storage devices.					
UNIT I	CRYSTAL STRUCTURE AND MATERIAL CHARACTERIZATION				9
Crystal structure – Unit cells – Crystal systems – Miller indices – Crystal defects – Point, line and surface defects – Atomic bonding – Structure-property relationship – X-ray diffraction (XRD) – Electron microscopy (SEM & TEM) – Energy dispersive spectroscopy (EDS) – Atomic Force Microscopy (AFM).					
UNIT II	ELECTRICAL, MAGNETIC AND DIELECTRIC MATERIALS				9
Electrical conduction in solids – Conductors, semiconductors and insulators – Dielectric materials – Polarization mechanisms – Ferroelectric materials – Piezoelectric materials – Ferrites – Soft and hard magnetic materials – Superconducting materials – Applications in electronic devices.					
UNIT III	SEMICONDUCTOR MATERIALS AND ELECTRONIC DEVICES				9
Elemental and compound semiconductors – Silicon, Germanium, GaAs, GaN, SiC – Crystal growth techniques – Zone refining – Czochralski method – Epitaxy – Wafer preparation – Oxidation – Diffusion – Ion implantation – Electronic packaging materials – Reliability issues.					
UNIT IV	NANOMATERIALS, THIN FILMS AND PHOTONIC MATERIALS				9
Introduction to nanomaterials – Carbon nanotubes – Graphene – Quantum dots – Thin film deposition techniques (PVD, CVD, ALD) – Transparent conducting oxides – Optical materials – Photonic crystals – MEMS materials – Flexible electronic materials – Electronic sensor materials.					
UNIT V	ADVANCED MATERIALS FOR ELECTRONICS				9
Wide bandgap semiconductors – Smart materials – Shape memory alloys – Multiferroic materials – Phase change materials – Energy materials for batteries and supercapacitors – Thermoelectric materials – Organic semiconductors – Materials for flexible electronics – Materials selection for AI hardware, sensors and photonic integrated circuits.					
ACTIVITIES:					
- Compare XRD, SEM, TEM and AFM techniques for characterization of semiconductor materials with suitable industrial applications. - Study the material selection and fabrication process of a modern CMOS integrated circuit or Wide Bandgap (SiC/GaN) power device.					

3. Mini report on Emerging materials for AI hardware, quantum computing, flexible electronics and next-generation photonic integrated circuit.
4. Review of GATE questions.

COURSE OUTCOMES:

- CO1:** Explain crystal structures, defects and characterization techniques used for electronic materials.
- CO2:** Analyze electrical, magnetic and dielectric properties of materials for electronic applications.
- CO3:** Evaluate semiconductor materials and fabrication processes used in electronic device manufacturing.
- CO4:** Apply nanomaterials, thin films and photonic materials in modern electronic systems.
- CO5:** Select suitable advanced functional materials for emerging electronic, sensing and energy applications.

TOTAL: 45 PERIODS

WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%

TEXTBOOKS:

1. William D. Callister Jr. & David G. Rethwisch, Materials Science and Engineering: An Introduction, 10th Edition, Wiley, 2020.
2. James F. Shackelford, Introduction to Materials Science for Engineers, 9th Edition, Pearson, 2023.

REFERENCES:

1. V. Raghavan, Materials Science and Engineering, 7th Edition, Prentice Hall India.
2. Donald R. Askeland & Wendelin J. Wright, The Science and Engineering of Materials, 8th Edition, Cengage Learning.
3. S. O. Kasap, Principles of Electronic Materials and Devices, 5th Edition, McGraw-Hill.
4. Y. Leng, Materials Characterization: Introduction to Microscopic and Spectroscopic Methods, 3rd Edition, Wiley.
5. B. G. Streetman & S. Banerjee, Solid State Electronic Devices, 8th Edition, Pearson.

CO's-PO's & PSO's MAPPING

Cos	PO1	PO2	PO3	PSO1	PSO2
CO1	3	2	-	3	2
CO2	3	3	2	3	2
CO3	3	3	3	3	3
CO4	2	3	3	3	3
CO5	2	3	3	3	3
AVG	2.6	2.8	2.2	3	2.6

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


Chairman
Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

AE26102	SENSORS, ACTUATORS AND INTERFACE ELECTRONICS	L	T	P	C
SDG: 9, 11		3	0	0	3

COURSE OBJECTIVES:

- Understand the principles, classification, and performance characteristics of measurement systems.
- Study the operating principles and signal conditioning techniques of resistive and reactive sensors.
- Analyze self-generating sensors and their signal conditioning circuits for accurate measurement.
- Study the operating principles and applications of mechanical, electromagnetic, and hydraulic actuators.
- Evaluate modern semiconductor, optical, biological, and intelligent sensors with microcontroller-based interfacing techniques.

UNIT I INTRODUCTION TO MEASUREMENT SYSTEMS

9

Introduction to measurement systems: general concepts and terminology – measurement systems, sensor classification – general input-output configuration, methods of correction – Performance characteristics: static characteristics and dynamic characteristics of measurement systems; zero-order – first-order – and second-order measurement systems and response.

UNIT II RESISTIVE AND REACTIVE SENSORS

9

Resistive sensor: potentiometers, strain gauges – resistive temperature detector (RTD) – Thermistors – magneto resistors – light-dependent resistors – Signal conditioning for resistive sensors: Wheatstone bridge – sensor bridge calibration and compensation – Reactive variation and electromagnetic sensors: capacitive sensors – inductive sensors – resistive sensors – Linear Variable Differential Transformers (LVDT) – application and signal conditioning of LVDT – magneto elastic sensors – hall effect sensors.

UNIT III SELF-GENERATING SENSORS

9

Self-generating sensors: thermoelectric sensors – piezoelectric sensors, pyroelectric sensors – photovoltaic sensors – electrochemical sensors – Signal conditioning for self-generating sensors: chopper and low-drift amplifiers – electrometer amplifiers – charge amplifiers – noise in charge amplifiers.

UNIT IV ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS

9

Relays, Solenoid drive – Stepper Motors – Voice-Coil actuators – Hydraulic actuators – Variable transformers: synchro-resolvers – Inductosyn – resolver-to-digital and digital-to-resolver converter.

UNIT V DIGITAL AND INTELLIGENT SENSORS

9

Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula – Machine interference Model – Steady State analysis – Self-service queue.

ACTIVITIES:

1. Prepare a technical report comparing RTD, Thermistor, Strain Gauge, LVDT, Hall Effect Sensor, and Capacitive Sensors.
2. Simulate thermocouple or piezoelectric sensor output characteristics using any Simulation Tools and plot the sensor output versus input stimulus.
3. Conduct a case study on IoT-enabled smart sensing systems used in healthcare, agriculture, or smart cities & Review of GATE Questions.
4. Review of GATE questions.

COURSE OUTCOMES:

CO1: Characterize the response properties of zero, first and second-order measurement systems.

CO2: Design signal conditioning and calibration circuits for resistive, capacitive and inductive sensors.

CO3: Implement precision instrumentation amplifiers for self-generating sensors.

CO4: Select, drive and evaluate electromechanical and hydraulic actuators including resolver interfaces.

CO5: Interface intelligent sensors and transducers with microcontroller communication protocols.

TOTAL: 45 PERIODS

WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%

TEXTBOOKS:

1. Ramon Pallas-Areny and John G. Webster, Sensors and Signal Conditioning, 3rd Edition, John Wiley & Sons, 2019.
2. John G. Webster and Halit Eren, (Eds.) Measurement, Instrumentation, and Sensors Handbook: Spatial, Mechanical, Thermal, and Radiation Measurement, 2nd Edition, CRC Press, 2022.

REFERENCES:

1. Jacob Fraden, Handbook of Modern Sensors: Physics, Designs, and Applications, 6th Edition, Springer, 2022.
2. Ernest O. Doebelin and Dhanesh N. Manik, Measurement Systems: Application and Design, 6th Edition, McGraw-Hill Education, 2019.
3. Clarence W. de Silva, Sensors and Actuators: Engineering System Instrumentation, 3rd Edition, CRC Press, 2023.
4. Walt Kester (Ed.), Data Conversion Handbook, 2nd Edition, Newnes (Elsevier), 2018.
5. Sergio M. Savaresi, Carlo Poussot-Vassal, Cristiano Spelta, Alberto Maria Savaresi and Luc Dugard, Semi-Active Suspension Control Design for Vehicles, Springer, Latest Edition.
6. Robert B. Northrop, Introduction to Instrumentation and Measurements, 4th Edition, CRC Press, 2021.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	2
CO2	3	1	3	3	3
CO3	3	1	3	3	3
CO4	2	1	3	3	2
CO5	3	2	3	3	3
AVG	2.6	1.2	3	2.8	2.6

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26103	ADVANCED DIGITAL SYSTEM DESIGN				L	T	P	C
SDG: 9, 12					3	0	0	3
COURSE OBJECTIVES:								
• To design asynchronous sequential circuits. • To learn about hazards in asynchronous sequential circuits. • To study the fault testing procedure for digital circuits. • To understand the architecture of programmable devices. • To design and implement digital circuits using programming tools.								
UNIT I	SEQUENTIAL CIRCUIT DESIGN							9
Analysis of Clocked Synchronous Sequential Circuits and Modelling- State Diagram, State Table, State Table Assignment and Reduction-Design of Synchronous Sequential Circuits Design of Iterative Circuits-ASM Chart and Realization using ASM.								
UNIT II	ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN							9
Analysis of Asynchronous Sequential Circuit – Flow Table Reduction-Races-State Assignment-Transition Table and Problems in Transition Table- Design of Asynchronous Sequential Circuit - Static, Dynamic and Essential hazards – Mixed Operating Mode Asynchronous Circuits – Designing Vending Machine Controller.								
UNIT III	FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS							9
Fault Table Method-Path Sensitization Method – Boolean Difference Method - D Algorithm — Tolerance Techniques – The Compact Algorithm – Fault in PLA – Test Generation - DFT Schemes – Built in Self-Test.								
UNIT IV	SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES							9
Programming Logic Device Families – Designing a Synchronous Sequential Circuit using PLA/PAL – Designing ROM with PLA – Realization of Finite State Machine using PLD – FPGA – Xilinx FPGA - Xilinx 4000.								
UNIT V	SYSTEM DESIGN USING VERILOG							9

Verilog HDL modeling, data types, behavioral & structural modeling, FSM synthesis, test benches, combinational/sequential circuit realization.

ACTIVITIES:

1. Design and simulate sequence detector, counters, and FSM using any Simulation Tools.
2. Analyze and eliminate static and dynamic hazards using any Simulation Tools.
3. Develop Verilog code for counters, FSMs and serial adders using any Simulation Tools.
4. Review of GATE Questions.

COURSE OUTCOMES:

CO1: Design basic digital circuits at the transistor level.

CO2: Select suitable logic styles for digital circuit design.

CO3: Analyze and optimize transistor-level digital circuits.

CO4: Evaluate and optimize the performance of digital circuits based on delay.

CO5: Explain the ASIC design flow, technology choices, and design methodologies.

TOTAL: 45 PERIODS

WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%

TEXTBOOKS:

1. Donald D. Givone, Digital Principles and Design, 2nd Edition, McGraw-Hill Education, Latest Reprint Edition.
2. Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, 3rd Edition, Pearson Education, 2020.

REFERENCES:

1. M. Morris Mano and Michael D. Ciletti, Digital Design, 6th Edition, Pearson Education, 2018.
2. Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with Verilog Design, 4th Edition, McGraw-Hill Education, 2021.
3. Charles H. Roth Jr. and Larry L. Kinney, Fundamentals of Logic Design, 8th Edition, Cengage Learning, 2021.
4. Michael D. Ciletti, Advanced Digital Design with the Verilog HDL, 2nd Edition, Pearson Education.
5. Neil H. E. Weste and David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th Edition, Pearson Education.
6. Steve Kilts, Advanced FPGA Design: Architecture, Implementation and Optimization, Wiley-IEEE Press.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	3	2
CO2	3	1	3	3	2
CO3	3	1	3	3	3
CO4	3	1	3	2	3
CO5	3	2	3	3	2
AVG	2.8	1.2	3	2.8	2.4

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


 Chairman
 Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

AE26104	IoT SYSTEM DESIGN AND SECURITY	L	T	P	C
SDG: 9, 7		3	0	2	4
COURSE OBJECTIVES:					
- To understand the evolution, architecture, and enabling technologies of the Internet of Things. - To analyze IoT middleware architectures, resource management techniques, and 5G-enabled IoT systems. - To study security, privacy, and trust issues in IoT smart ambient systems. - To investigate IoT communication protocols, standards, and their security implications. - To design and analyze IoT-based applications for smart environments and industrial systems.					
UNIT I	INTRODUCTION TO INTERNET OF THINGS				9
Rise of the machines – Evolution of IoT – Web 3.0 view of IoT – Definition and characteristics of IoT – Physical design of IoT – Logical design of IoT – IoT enabling technologies – IoT levels and deployment templates – Applications view of IoT applications.					
UNIT II	ARCHITECTURE OF IoT				9
IoT architecture – IoT ecosystem – Identification and addressing of IoT devices – Naming and discovery of IoT objects and services – Middleware architecture for IoT – Service-Oriented Architecture (SOA) for IoT – Middleware for RFID, Wireless Sensor Networks (WSN), SCADA and Machine-to-Machine (M2M) communication – Resource management in IoT – Introduction to 5G-enabled IoT architecture – Applications of IoT in smart electronics and industrial automation.					
UNIT III	SECURITY CONSIDERATIONS IN IoT SMART AMBIENT SYSTEMS				9
Security in Smart Grids and Smart Spaces for Smooth IoT Deployment in 5G (5G and the Internet of Things-Smart Spaces-Smart Grids Security and Privacy – Services that Need to Be Secure – Security Requirements – Security Attack-Security Measures and Ongoing Research) – Security Challenges in 5G-Based IoT Middleware Systems (Security in 5G-Based IoT Middleware-Security Challenges Toward 5G).					
UNIT IV	IoT-ENABLERS AND THEIR SECURITY AND PRIVACY ISSUES				9
Internet of Things layer wise Protocols and Standards – EPC global architecture, specifications, identity adaptation, security and vulnerabilities, advantages and disadvantages – Wireless HART – Zigbee – Near Field Communication – 6LoWPAN-DASH7-Comparative Analysis.					
ACTIVITIES: Prepare a comparative chart of ZigBee, NFC, RFID, WirelessHART, DASH7, and 6LoWPAN protocols & Review of GATE questions.					
UNIT V	APPLICATIONS AND CASE STUDIES				9
Home automation – Smart cities – Environment – Energy – Retail – Logistics – Agriculture – Industry – Health and life style – Case study.					
ACTIVITIES:					
- Mini-Presentation on a cyberattack scenario in a smart grid and propose suitable counter measures. - Prepare a comparative chart of ZigBee, NFC, RFID, WirelessHART, DASH7, and 6LoWPAN protocols. - Review of GATE questions.					
					45 PERIODS
LIST OF EXPERIMENTS:					30 PERIODS
- Study of IoT architecture, physical and logical design using simulation tools. - Design and implementation of an IoT deployment model for smart monitoring. - Simulation of IoT middleware architecture and resource discovery mechanisms. - Implementation of MQTT/CoAP communication for IoT devices - Analysis of 5G-enabled IoT communication and middleware services. - Security vulnerability assessment of IoT devices and networks. - Implementation of authentication and encryption techniques in IoT systems. - Comparative study of ZigBee, NFC, and 6LoWPAN protocols. - RFID and EPCglobal-based object identification system implementation. - Smart Home Automation using NodeMCU/ESP32 and cloud platform. - IoT-based Smart Agriculture Monitoring System.					

12. Mini Project: Design of an IoT Application with Security Features.

COURSE OUTCOMES:

CO1: Explain the concepts, architecture, and enabling technologies of IoT systems.

CO2: Analyze IoT architectures, middleware, and resource management techniques.

CO3: Evaluate security and privacy issues in IoT systems.

CO4: Compare IoT communication protocols and standards for different applications.

CO5: Design IoT-based solutions for smart and industrial applications.

TOTAL: 75 PERIODS

WEIGHTAGE: Continuous Assessment: 50%, End Semester Examinations: 50%

TEXTBOOKS:

1. Arshdeep Bahga and Vijay Madisetti, Internet of Things – A Hands-on Approach, 2nd Edition, Universities Press, 2023.

2. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton and Jerome Henry, IoT Fundamentals: Networking Technologies, Protocols and Use Cases for the Internet of Things, 2nd Edition, Cisco Press, 2023.

REFERENCES:

1. Adrian McEwen and Hakim Cassimally, Designing the Internet of Things, 2nd Edition, Wiley, 2023.

2. Olivier Hersent, David Boswarthick and Omar Elloumi, The Internet of Things: Key Applications and Protocols, 3rd Edition, Wiley, 2022.

3. Rajkumar Buyya and Amir Vahid Dastjerdi (Editors), Internet of Things: Principles and Paradigms, 2nd Edition, Morgan Kaufmann (Elsevier), 2024.

4. Pethuru Raj and Anupama C. Raman, The Internet of Things: Enabling Technologies, Platforms and Use Cases, CRC Press, Latest Edition.

5. Fei Hu, Security and Privacy in Internet of Things (IoTs): Models, Algorithms and Implementations, CRC Press, Latest Edition.

6. Andrew Minter, Analytics for the Internet of Things (IoT): Intelligent Analytics for Your Intelligent Devices, Packt Publishing, Latest Edition.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	2
CO2	3	1	3	3	3
CO3	3	2	3	3	3
CO4	2	2	3	3	2
CO5	3	2	3	3	3
AVG	2.6	1.6	3	2.8	2.6

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


Chairman
Board of Studies
Department of Electronics and Communication Engineering
Kingston Engineering College
Vellore - 632 059

AE26105		STATISTICAL SIGNAL PROCESSING AND MODELING	L	T	P	C
SDG: 9, 3			2	0	2	3
COURSE OBJECTIVES:						
- To understand the fundamentals of random processes and statistical signal processing. - To develop mathematical models for stochastic signals using AR, MA, and ARMA techniques. - To analyze and estimate power spectra using parametric and non-parametric methods. - To design optimum linear estimators and Wiener filters for signal enhancement. - To implement adaptive filtering algorithms for estimation, equalization, and noise cancellation applications.						
UNIT I		INTRODUCTION TO RANDOM SIGNAL PROCESSING				6
Discrete random processes, ensemble averages, stationarity, bias & estimation, autocovariance, autocorrelation, Parseval's theorem, Wiener-Khintchine relation, white noise, PSD, spectral factorization, filtering						
UNIT II		SIGNAL MODELING				6
AR, MA, ARMA models, forward-backward linear prediction, Yule-Walker method, Prony's equations, Levinson-Durbin algorithm.						
UNIT III		SPECTRAL ESTIMATION				6
Spectral Estimation: Spectral estimation from finite signals, nonparametric methods (periodogram, Bartlett, Welch, Blackman-Tukey), parametric methods, AR spectral estimation, harmonic detection.						
UNIT IV		LINEAR ESTIMATION				6
LMMSE filtering, Wiener-Hopf equations, FIR/IIR Wiener filters, causation & estimation, noise cancellation.						
UNIT V		ADAPTIVE FILTERS				6
FIR adaptive filters, steepest descent, LMS, normalized LMS, RLS algorithm, adaptive equalization, echo & noise cancellation.						
ACTIVITIES:						
- Prepare a mini report on real-world application of random signal processing such as wireless fading channels, speech signals, and biomedical signals - Mini-Presentation on the application of linear prediction in speech processing and time-series forecasting. - Review of GATE questions.						
30 PERIODS						
LIST OF EXPERIMENTS:		30 PERIODS				
- Simulate discrete random processes in MATLAB/Python. - PSD estimation via periodogram, autocorrelation & FFT for sample signals. - Perform AR, MA, ARMA model using time-series data. - Implement forward and backward prediction. - Apply periodogram, Bartlett, and Blackman-Tukey methods on signals. - Detect harmonic components using AR spectral estimation. - Design FIR and IIR Wiener filters in MATLAB/Python. - Solve Wiener-Hopf equations for given signals. - Design FIR and IIR Wiener filters in MATLAB/Python. - Solve Wiener-Hopf equations for given signals.						
COURSE OUTCOMES:						
CO1: Explain the concepts of random processes and their statistical properties.						
CO2: Develop signal models using AR, MA, and ARMA techniques.						
CO3: Apply spectral estimation techniques for signal analysis.						
CO4: Design Wiener filters for signal estimation and noise reduction.						
CO5: Implement adaptive filtering algorithms for practical signal processing applications.						
TOTAL: 60 PERIODS						

WEIGHTAGE: Continuous Assessment: 50%, End Semester Examinations: 50%

TEXTBOOKS:

1. Monson H. Hayes, Statistical Digital Signal Processing and Modeling, 1st Edition, John Wiley & Sons, Latest Reprint Edition, 2022.
2. Steven M. Kay, Fundamentals of Statistical Signal Processing: Estimation Theory, Volume I, Prentice Hall, Latest Reprint Edition, 2021.

REFERENCES:

1. Steven M. Kay, Modern Spectral Estimation: Theory and Application, Classic Edition, Pearson Education / Prentice Hall, Latest Reprint.
2. Simon Haykin, Adaptive Filter Theory, 5th Edition, Pearson Education, Latest Reprint Edition.
3. Sophocles J. Orfanidis, Optimum Signal Processing: An Introduction, 3rd Edition, McGraw-Hill Education, Latest Reprint.
4. Ali H. Sayed, Fundamentals of Adaptive Filtering, Wiley-IEEE Press, Latest Reprint Edition.
5. Alan V. Oppenheim, Ronald W. Schaffer and John R. Buck, Discrete-Time Signal Processing, 3rd Edition, Pearson Education, Latest Reprint.
6. Petre Stoica and Randolph Moses, Spectral Analysis of Signals, Pearson/Prentice Hall, Latest Reprint Edition.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	2
CO2	3	1	3	3	3
CO3	3	2	3	3	3
CO4	3	2	3	3	3
CO5	3	2	3	3	3
AVG	2.8	1.6	3	2.8	2.8

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


Chairman
Board of Studies
Department of Electronics and Communication Engineering
Kingston Engineering College
Vellore - 632 059

AE26111	ELECTRONIC SYSTEM DESIGN LABORATORY	L	T	P	C
SDG: 4, 9		0	0	4	2

COURSE OBJECTIVES:

- Understand the characteristics and operation of various sensors and actuators used in electronic systems.
- Design and implement signal conditioning and interface circuits for sensor-based applications.
- Analyze and design analog electronic circuits using operational amplifiers and analog ICs.
- Interface sensors and actuators with embedded controllers for monitoring and control applications.
- Develop complete electronic systems integrating sensors, analog interfaces, actuators, and embedded platforms.

LIST OF EXPERIMENTS:

- I. Sensors and Signal Conditioning:**
 1. Characteristics and calibration of temperature sensors (RTD, Thermistor and LM35).
 2. Design and implementation of Wheatstone bridge and instrumentation amplifier for sensor measurements.
 3. Interfacing and characterization of LDR and Hall-effect sensors.
 4. Design of active signal conditioning circuits for low-level sensor outputs.
- II. Interface Electronics:**
 5. Design and implementation of Analog-to-Digital Converter (ADC) interfacing circuit.
 6. Design and implementation of Digital-to-Analog Converter (DAC) interfacing circuit.
 7. Design of active low-pass, high-pass and band-pass filters for sensor applications.
- III. Analog IC Design:**
 8. Design and analysis of Op-Amp based precision rectifier and comparator circuits.
 9. Design and implementation of Schmitt Trigger and waveform generation circuits.
 10. Design and simulation of Phase Locked Loop (PLL) applications using analog ICs.
- IV. Actuator Interfacing:**
 11. Interfacing and speed control of DC motor using driver circuits.
 12. Stepper motor interfacing and position control using microcontroller.
 13. Servo motor control using PWM techniques and relay/solenoid interfacing.
- V. System Design Experiments:**
 14. Design and implementation of sensor-to-cloud monitoring system using ESP32/NodeMCU.
 15. Mini Project: Development of an Electronic System integrating Sensors, Interface Electronics, Analog ICs and Actuators.

60 PERIODS

WEIGHTAGE: Continuous Assessment: 60%, End Semester Examinations: 40%

COURSE OUTCOMES:

- CO1:** Analyze and characterize sensors and actuators for measurement and control applications.
CO2: Design and implement signal conditioning and interface circuits for sensor systems.
CO3: Design and evaluate analog circuits using operational amplifiers and analog ICs.
CO4: Develop embedded systems for sensor acquisition and actuator control.
CO5: Design and realize integrated electronic systems for real-world applications.

LAB REQUIREMENTS:

HARDWARE REQUIREMENTS:

1. Desktop Computers (i5/i7, 8 GB RAM) - 15 Nos.
2. Digital Storage Oscilloscopes (100 MHz or above) - 10 Nos.
3. Function Generators - 10 Nos.
4. Regulated DC Power Supplies - 10 Nos.
5. Digital Multimeters - 15 Nos.
6. Breadboards and Prototyping Kits - 15 Sets
7. Arduino UNO Boards - 10 Nos.
8. ESP32 / NodeMCU Development Boards - 10 Nos.
9. DC Motor and Driver Modules - 10 Sets
10. Stepper Motor and Driver Kits - 10 Sets

[Signature]
Chairman

Board of Studies

Department of Electronics and Communication Engineering
Kingston Engineering College
Vellore - 632 059

11. Servo Motors - 10 Nos.
12. Relay and Solenoid Modules - 10 Nos.
13. RTD, Thermistor and LM35 Sensors - 10 Sets
14. Hall Effect Sensors - 10 Nos.
15. LDR Sensors - 10 Nos.
16. Instrumentation Amplifier ICs (AD620/TNA128) - 20 Nos.
17. Op-Amps (LM741, LM358, TL081) - 50 Nos.
18. PLL ICs (CD4046/LM565) - 20 Nos.
19. ADC and DAC Evaluation Kits - 10 Sets
20. Electronic Component Kit (R, L, C, Diodes, Transistors) - 15 Sets

SOFTWARE REQUIREMENTS:

1. MATLAB/SciLAB and Simulink
2. LT Spice
3. Multisim
4. Proteus Design Suite
5. Arduino IDE
6. Python (NumPy, SciPy, Matplotlib)
7. KiCad / EasyEDA PCB Design Software
8. LabVIEW (Optional)
9. Cadence Virtuoso (Optional)

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	2
CO2	3	1	3	3	2
CO3	3	1	3	3	2
CO4	3	1	2	3	3
CO5	3	2	3	3	3
AVG	2.8	1.2	2.8	2.8	2.4

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


 Chairman
 Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

SEMESTER II

AE26201	DIGITAL CMOS VLSI DESIGN	L	T	P	C
SDG: 9, 7		3	0	0	3
COURSE OBJECTIVES: - To introduce the basic concepts of MOS transistors. - To introduce the basic concepts of CMOS Technologies. - To provide a platform for transistor level digital circuits design. - To learn and practice different logical implementation and their significances. - To understanding of issues and tools related to ASIC design and implementation.					
UNIT I	MOSFET AND CMOS INVERTER	9			
MOSFET: Device Structure and Physical Operation – Current-Voltage (I-V) Characteristics – Scaling – Non-ideal Features of MOS Transistors – MOSFET Capacitances – MOSFET SPICE Models CMOS Inverter: Circuit Operation - The Voltage-Transfer Characteristic - Dynamic Operation - Power Dissipation – Layout.					
UNIT II	CMOS PROCESSING TECHNOLOGY, DELAY AND POWER	9			
CMOS Processing Technology: CMOS Technologies, Layout Design Rules, CMOS Process Enhancements. Delay: Propagation Delays and Delay Models – Logic Effort - Path-Delay Optimization. Power: Static Power Dissipation - Dynamic Power Dissipation - Power and Delay Trade-offs -Low Power Designs.					
UNIT III	COMBINATIONAL LOGIC CIRCUIT DESIGN	9			
Static CMOS Logic Circuits: NAND Gate – NOR Gate – Complex Logic Gates; Sizing Gates – Transmission Gate - Pseudo-nMOS Logic; Dynamic CMOS Logic Circuits: Basic Dynamic Logic – Non-ideal Effects of Dynamic Logic - Domino Logic.					
UNIT IV	SEQUENTIAL LOGIC CIRCUIT DESIGN AND DATA PATH SUB SYSTEMS DESIGN	9			
Static Latches and Registers - Dynamic Latches and Registers - Alternative Register Styles, Pipelining - Nonbistable Sequential Circuits. Datapath Subsystem Designs: Architectures for Adders, Multipliers, Shifters.					
UNIT V	IMPLEMENTATION OPTIONS AND INTERCONNECT	9			
Implementation Options: Platform based systems – ASICs – Field Programmable Devices – Design Flow Interconnect: RLC Parasitic, Interconnect Models – Parasitic Effects of Interconnects.					
ACTIVITIES: - Case study on low-power CMOS techniques used in mobile processors - Design and simulate CMOS NAND, NOR and Domino logic circuits and compare performance using any simulation tools. - Prepare a Mini-Report on interconnect parasitics and signal integrity issues - Review of GATE Questions.					
COURSE OUTCOMES: CO1: Design basic digital circuits in transistor level. CO2: Analyze and choose suitable logical styles for a given problem. CO3: Analyze and optimize the transistor level circuits. CO4: Measure the delay, analyze and find the optimized delay. CO5: Understand the ASIC design flow and technology selection.					
TOTAL: 45 PERIODS					
WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%					
TEXTBOOKS: Neil H. E. Weste and David Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, 4th Edition, Pearson Education. (Unit I to V)					

2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective", 2nd Edition, Pearson Education. (Unit I to V)

REFERENCES:

1. Sung-Mo (Steve) Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 4th Edition, McGraw-Hill Education, 2021.
2. John P. Uyemura, Introduction to VLSI Circuits and Systems, 2nd Edition, Wiley India, Latest Reprint.
3. Neil H. E. Weste and David Harris, ASIC Design: A Practical Guide to Verilog-Based Design, Pearson Education, Latest Edition.
4. M. J. Smith, Application-Specific Integrated Circuits (ASICs), Addison-Wesley, Latest Reprint Edition.
5. Wayne Wolf, Modern VLSI Design: System-on-Chip Design, 4th Edition, Pearson Education, Latest Reprint.
6. Douglas A. Pucknell and Kamran Eshraghian, Basic VLSI Design, 3rd Edition, Prentice Hall India, Latest Reprint.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	3	2
CO2	2	1	3	3	2
CO3	3	1	3	3	3
CO4	3	1	3	2	3
CO5	3	2	3	3	2
AVG	2.6	1.2	3	2.8	2.4

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26202	EMBEDDED SYSTEM DESIGN				L	T	P	C
SDG: 11, 9					3	0	2	4

COURSE OBJECTIVES:

- To expose the students to the fundamentals of embedded system design.
- To enable the students to understand and use embedded computing platform.
- To introduce networking principles in embedded devices.
- To learn real time characteristics in embedded system design.
- To explore system design techniques.

UNIT I	EMBEDDED PROCESSORS	9
Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Design Example: Model Train Controller, ARM processor- processor and memory organization.		
UNIT II	EMBEDDED COMPUTING PLATFORM	9
Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example: Alarm Clock		
UNIT III	NETWORKS	9
Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I ² C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network- Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.		
UNIT IV	REAL-TIME CHARACTERISTICS	9

Clock driven Approach, weighted Round Robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off- line Versus Online scheduling.

UNIT V SYSTEM DESIGN TECHNIQUES

9

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

ACTIVITIES:

1. Prepare a detailed block diagram illustrating ARM/SHARC processor interfacing with memory, I/O devices, buses, and peripherals.
2. Analyze the communication architecture of an embedded system such as an automotive CAN network, industrial automation system, or smart home IoT network using I²C, CAN, Ethernet, or SPI.
3. Review of GATE questions.

45 PERIODS

LIST OF EXPERIMENTS:

30 PERIODS

1. Push button, LED, LCD display and RTC interfacing with AVR RISC based microcontroller.
2. AVR RISC based Microcontroller system design with Touch screen interfacing.
3. Motor (DC, stepper, servo) interfacing with AVR RISC based Microcontroller.
4. Interfacing sensors and RFID with AVR RISC based Microcontroller.
5. Design of RC5 remote control decoder with AVR RISC based Microcontroller.
6. Implementing I2C, SPI, CAN and UART protocols with ARM 7 processor.
7. Design and implementation of path tracking and obstacle avoidance Robot.
8. Design and implementation of self-balancing Robot.
9. Design and implementation of Robotic Arm manipulation with 6 DOF.
10. Design and implementation of Pick and Place robot.
11. Design and implementation of color and pattern guided material handling robot.
12. Design and implementation of human detection robot using PIR sensor.

COURSE OUTCOMES:

CO1: Explore fundamentals of embedded system design.

CO2: Interpret and use embedded computing platform.

CO3: Apply networking principles in embedded devices.

CO4: Gain insight on the characteristics in embedded system design.

CO5: Design embedded systems for real-world applications using RTOS, sensors, memory, and communication interfaces.

TOTAL: 75 PERIODS

WEIGHTAGE: Continuous Assessment: 50%, End Semester Examinations: 50%

TEXTBOOKS:

1. Marilyn Wolf, Computers as Components: Principles of Embedded Computing System Design, 4th Edition, Morgan Kaufmann (Elsevier), 2023.
2. (Comprehensive coverage of embedded processors, ARM architecture, hardware/software co-design, embedded networking, and system design.)
3. Jonathan W. Valvano, Embedded Systems: Real-Time Interfacing to ARM Cortex-M Microcontrollers, 5th Edition, Cengage Learning, 2023.

REFERENCES:

1. Shibu K. V., Introduction to Embedded Systems, 3rd Edition, McGraw-Hill Education, 2024.
2. Frank Vahid and Tony Givargis, Embedded System Design: A Unified Hardware/Software Introduction, 3rd Edition, Wiley India, Latest Edition.
3. Raj Kamal, Embedded Systems: Architecture, Programming and Design, 4th Edition, McGraw-Hill Education, 2023.

(Signature)
Chairman

Board of Studies

Department of Electronics and Communication Engineering
Kingston Engineering College
Vellore - 632 059

4. Muhammad Ali Mazidi, Sarmad Naimi and Sepehr Naimi, ARM Microcontroller Programming and Interfacing, Latest Edition, Pearson Education.
5. Jane W. S. Liu, Real-Time Systems, 2nd Edition, Pearson Education, Latest Reprint.
6. Qing Li and Caroline Yao, Real-Time Concepts for Embedded Systems, 2nd Edition, CMP Books, Latest Reprint.

Joseph Yiu, The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors, 3rd Edition, Newnes (Elsevier), 2020.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	2
CO2	3	1	3	3	2
CO3	3	1	3	2	3
CO4	2	1	3	2	2
CO5	3	2	3	3	3
AVG	2.6	1.2	3	2.4	2.4

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26211	ANALOG AND DIGITAL CMOS VLSI DESIGN	L	T	P	C
SDG: 9, 4	LABORATORY	0	0	4	2

COURSE OBJECTIVES:

- To understand operation of NMOS and PMOS devices.
- To get familiar with the small- and large-signal models of NMOS and PMOS transistors.
- To understand the concept of gain and Transconductance of Transistors.
- Students will carry out a detailed analog circuit design starting with transistor characterization and finally realizing an IA design.
- At various stages of design, a typical state of art CAD VLSI tool will be used in various phases of experiments designed to bring out the key aspects of each important module in the CAD tool including the simulation, layout, LVS and parasitic extracted simulation.

LIST OF EXPERIMENTS:

(1) Extraction of process parameters of CMOS process transistors

1. Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
2. Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine V_t .
3. Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
4. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
5. Extract V_{th} of NMOS/PMOS transistors (short channel and long channel). Use VDS of appropriate voltage to extract V_{th} use the following procedure.
 - (i) Plot gm vs VGS using SPICE and obtain peak gm point.
 - (ii) Plot $y=ID/(gm)$ as a function of VGS using SPICE.
 - (iii) Use SPICE to plot tangent line passing through peak gm point in y (VGS)
6. Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it

(2) CMOS inverter design and performance analysis

1. (i) Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
- (ii) Plot VTC for CMOS inverter with varying VDD.
- (iii) Plot VTC for CMOS inverter with varying device ratio.

Board of Studies

Department of Electronics and Communication Engineering
Kingston Engineering College
Vellore - 632 059

2. Perform transient analysis of CMOS inverter with no load and with load and determine t_{pHL} , t_{pLH} , 20%-to-80% t_r and 80%-to-20% t_f .

3. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.

(3) Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.

(4) Single stage amplifier design and performance analysis

1. Draw small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors
2. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load:
 - (i) Establish a test bench to achieve $V_{DSQ} = V_{DD}/2$
 - (ii) Calculate input bias voltage for a given bias current
 - (iii) Use spice and obtain the bias current. Compare with the theoretical value
 - (iv) Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in spice, considering load capacitance
 - (v) Plot step response of the amplifier with a specific input pulse amplitude. Derive time constant of the output and compare it with the time constant

(5) Three OPAMP Instrumentation Amplifier.

1. Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
 - (i) Draw the schematic of op-amp macro model.
 - (ii) Draw the schematic of INA.
 - (iii) Obtain parameters of the op-amp macro model such that it meets a given specification for: (i) low-frequency voltage gain, (ii) unity gain BW (f_u), (iii) input capacitance (iv) output resistance & (v) CMRR
2. Draw schematic diagram of CMRR simulation setup
3. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
4. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches

(6) Use Layout editor.

1. Draw layout of a minimum size inverter using transistor from CMOS process library. Use Metal 1 as interconnect line between inverters.
2. Run DRC, LVS and RC extraction. Make sure there is no DRC error.
3. Extract the netlist. Use extracted netlist and obtain t_{pHL} , t_{pLH} for the inverter using Spice.
4. Use a specific interconnect length and connect and connect three inverters in a chain.
5. Extract the new netlist and obtain t_{pHL} and t_{pLH} of the middle inverter
6. Compare new values of delay times with corresponding values obtained in part '3'.

(7) Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter:

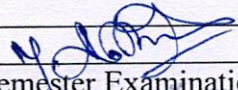
- (i) low-frequency voltage gain
- (ii) unity gain BW (f_u)
- (iii) Power dissipation
- (iv) Perform DC analysis and determine input common mode range and compare with the theoretical values
- (v) Perform time domain simulation and verify low frequency gain.
- (vi) Perform AC analysis and verify.

60 PERIODS

WEIGHTAGE: Continuous Assessment: 60%, End Semester Examinations: 40%

COURSE OUTCOMES:

CO1: Design basic digital and analog CMOS circuits.


 Chairman
 Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

CO2: Analyze the time-domain performance of analog CMOS circuits.

CO3: Analyze the frequency-domain performance of analog CMOS circuits.

CO4: Use EDA tools to design and simulate CMOS circuits.

CO5: Explain the operation and performance of CMOS inverters and differential amplifiers.

LAB REQUIREMENTS:

1. High Performance Workstations (Core i7/i9, 16 GB RAM, 1 TB SSD) - 10 Nos. (One setup for three students)
2. Cadence Virtuoso Design Environment - 10 Licenses
3. Cadence Spectre Circuit Simulator - 10 Licenses
4. Cadence Assura / Pegasus DRC-LVS Verification Tool - 10 Licenses
5. Cadence Quantus RC Extraction Tool - 10 Licenses
6. Synopsys HSPICE / PrimeSim Simulator - 5 Licenses
7. CMOS Process Design Kit (180 nm / 130 nm CMOS Technology) - 1 Set
8. Layout Editor with DRC/LVS Support - 10 Licenses
9. Analog Design Environment (ADE) - 10 Licenses
10. Waveform Analysis Tool (ViVA / EZWave) - 10 Licenses
11. FFT and Spectrum Analysis Utility - 10 Licenses
12. MATLAB / Python Scientific Computing Environment - 10 Installations
13. Central CAD License Server - 1 No.
14. Gigabit Ethernet Network Switch - 1 No.
15. Laser Printer & LCD Projector - 1 No.
16. UPS Backup Facility (5 kVA or higher) - 1 Setup

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	3	1	3	3	2
CO2	3	1	3	2	3
CO3	3	1	3	2	3
CO4	2	1	2	3	3
CO5	2	2	3	2	2
AVG	2.6	1.2	3	2.4	2.6

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


Chairman
Board of Studies
Department of Electronics and Communication Engineering
Kingston Engineering College
Vellore - 632 059

AE26S02	TECHNICAL SEMINAR AND RESEARCH COMMUNICATION	L	T	P	C
SDG: 4, 9		0	0	2	2

COURSE OBJECTIVES:

- Understand the principles of technical communication and professional presentation.
- Develop effective literature search, review and critical analysis skills using scholarly databases.
- Identify a research problem and prepare a technically sound survey/term paper.
- Enhance scientific writing, referencing and publication ethics.
- Improve technical presentation, communication and discussion skills required for research and industry.

Weeks	Topics	Evaluation
Week 1	Course orientation, importance of technical communication, seminar planning, selection of research area and guide allocation.	5% - Topic Selection & Objectives
Week 2	Identification of research topic, formulation of objectives, scope and problem statement.	
Week 3	Literature survey using IEEE Xplore, ScienceDirect, Springer, Google Scholar and Scopus; Reference management tools.	10% - Literature Survey & Bibliography
Week 4	Collection and classification of research papers (minimum 20 papers); preparation of annotated bibliography.	
Week 5	Critical analysis of selected papers; identification of research gaps and future scope.	10% - Research Gap Identification
Week 6	Preparation and delivery of Seminar-I based on literature review; peer discussion and evaluation.	15% - Seminar-I Presentation
Week 7	Preparation of survey framework, paper organization and chapter outline.	15% - Draft Survey Paper
Week 8	Technical writing: Abstract, Introduction, Related Work, Methodology, Comparative Analysis, Conclusion and References (IEEE format).	
Week 9	Research ethics, plagiarism, copyright, citation styles, publication ethics and AI-assisted writing guidelines.	
Week 10	Draft submission of survey/term paper and faculty review.	
Week 11	Revision based on review comments, preparation of final manuscript and plagiarism verification.	40% - Final Survey/Term Paper, Seminar-II & Viva-Voce
Week 12	Seminar-II: Presentation of survey paper, research gap, proposed future work and viva-voce.	
Week 13	Final submission of survey paper/term paper and presentation slides.	5% - Attendance, Participation & Professional Conduct
Week 14 & Week 15	Comprehensive evaluation, viva-voce and course wrap-up.	

30 PERIODS

WEIGHTAGE: Continuous Assessment: 100%, End Semester Examinations: 0%

COURSE OUTCOMES:

CO1: Identify a research problem and conduct a literature survey.

CO2: Analyze research papers and identify research gaps.

CO3: Prepare a technical paper using standard scientific writing practices.

CO4: Deliver effective technical seminar presentations.

CO5: Follow research ethics, publication ethics, and proper citation practices.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	3	1	2	2	3
CO2	3	2	3	1	2
CO3	3	2	3	2	3
CO4	2	3	3	1	2
CO5	1	3	2	1	1
AVG	2.4	2.2	2.6	1.4	2.2

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


Chairman
Board of Studies
Department of Electronics and Communication Engineering
Kingston Engineering College
Vellore - 632 059

SEMESTER III

AE26301	DIGITAL IMAGE AND VIDEO PROCESSING	L	T	P	C
SDG: 9, 3		3	0	2	4
COURSE OBJECTIVES:					
- Understand the fundamentals of digital image and video processing techniques. - Analyze motion estimation, video representation, and compression methods. - Apply image analysis, object tracking, and 3D reconstruction techniques. - Evaluate deep learning approaches for image and video analysis. - Design real-time image and video processing systems for intelligent applications.					
UNIT I	MOTION ESTIMATION AND VIDEO FUNDAMENTALS				9
Temporal vs. spatial image processing - Basics of video formation and representation (color video, interlaced vs. progressive) - Frame differencing and background subtraction - Block matching algorithms (Full Search, Three Step Search, Diamond Search) - Optical flow (Lucas-Kanade and Horn-Schunck methods) - Applications: surveillance, object tracking.					
UNIT II	VIDEO COMPRESSION STANDARDS AND TECHNIQUES				9
Temporal redundancy and inter-frame coding - Overview of video compression standards: MPEG-1/2/4, H.264/AVC, HEVC - Intra vs. inter coding, GOP structure - Motion compensation and entropy coding in video codecs - Scalable and Multiview video coding.					
UNIT III	3D IMAGE PROCESSING AND MULTIVIEW VIDEO				9
Stereoscopic imaging and disparity map estimation - 3D reconstruction from multiple images - Structure from motion (SfM) - Multiview video systems and depth estimation - Applications in VR/AR and 3D television.					
UNIT IV	ADVANCED IMAGE AND VIDEO ANALYSIS				9
Video segmentation and object tracking (Kalman filter, mean-shift, particle filter) - Action and gesture recognition - Scene understanding and semantic segmentation - Face and emotion recognition in video - Deep learning applications: CNNs for video, 3D CNNs, RNNs/LSTMs.					
UNIT V	REAL-TIME PROCESSING AND APPLICATIONS				9
Real-time image/video processing architectures (GPU, FPGA) - Edge AI and deployment on embedded devices - High-speed video capture and analysis - Applications: autonomous driving, medical video analysis, drone surveillance - Case studies and open research challenges.					
ACTIVITIES:					
- Compare block matching and optical flow techniques for motion estimation using OpenCV. - Analyze H.264, MPEG-4 and HEVC codecs using FFmpeg and compare compression efficiency. - Review of GATE questions.					
45 PERIODS					
LIST OF EXPERIMENTS:		30 PERIODS			
- Implement and compare block matching and optical flow algorithms (Lucas-Kanade & Farneback) on test videos using OpenCV (Python) & UCF101 dataset. - Pre-class video lectures + in-class implementation of MOG2 and KNN background subtraction on surveillance footage using OpenCV & Code samples from GitHub. - Encode videos using H.264, MPEG-4, and HEVC: Evaluate size, PSNR, and SSIM using FFmpeg (open source). - Analyze Group of Pictures (GOP) in compressed video streams using Handbrake, OpenCV & Python. - Compute disparity maps from stereo pairs and visualize depth using OpenCV stereo block matching & Middlebury Stereo Dataset. - Reconstruct sparse and dense 3D scenes from multiple views using COLMAP (open source SfM) & ETH3D dataset. - Use pretrained 3D CNN + LSTM pipeline to classify video actions using PyTorch or TensorFlow & UCF101 dataset.					

8. Deploy real-time object tracker on edge device using OpenCV + YOLOv5 or MobileNet-SSD.

COURSE OUTCOMES:

CO1: Explain the fundamentals of digital image and video processing.

CO2: Apply motion estimation and video compression techniques.

CO3: Analyze 3D image processing and Multiview video systems.

CO4: Evaluate deep learning methods for image and video analysis.

CO5: Design real-time image and video processing systems for intelligent applications.

TOTAL: 75 PERIODS

WEIGHTAGE: Continuous Assessment: 50%, End Semester Examinations: 50%

TEXTBOOKS:

1. Rafael C. Gonzalez and Richard E. Woods, Digital Image Processing, 4th Edition, Pearson Education, 2018.
2. A. Murat Tekalp, Digital Video Processing, 2nd Edition, Prentice Hall / Pearson, Latest Reprint.

REFERENCES:

1. Richard Szeliski, Computer Vision: Algorithms and Applications, 2nd Edition, Springer, 2022.
2. Mark Nixon and Alberto Aguado, Feature Extraction and Image Processing for Computer Vision, 4th Edition, Academic Press (Elsevier), 2020.
3. Alan C. Bovik (Ed.), The Essential Guide to Image and Video Processing, 2nd Edition, Academic Press, Latest Reprint.
4. David Forsyth and Jean Ponce, Computer Vision: A Modern Approach, 2nd Edition, Pearson Education.
5. Adrian Kaehler and Gary Bradski, Learning OpenCV 4: Computer Vision with OpenCV Library, 2nd Edition, O'Reilly Media, 2019.
6. Ian Goodfellow, Yoshua Bengio and Aaron Courville, Deep Learning, MIT Press, Latest Reprint.

CO's-PO's & PSO's MAPPING

COs	PO1	PO2	PO3	PSO1	PSO2
CO1	3	2	–	3	2
CO2	3	3	2	3	2
CO3	3	3	3	3	3
CO4	2	3	3	3	3
CO5	2	3	3	3	3
AVG	2.6	2.8	2.2	3	2.6

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


Chairman
 Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

PROGRAMME ELECTIVES

AE26001	NANO ELECTRONICS AND TECHNOLOGY				L	T	P	C
SDG: 9, 3, 7, 13					3	0	0	3
COURSE OBJECTIVES: • To understand the basic modelling of quantum mechanics. • To understand various advanced concepts in nanoelectronics. • To understand the synthesis of Nano materials. • To understand the characterization methods of Nano materials. • To understand Nano electronic devices and their applications.								
UNIT I	FUNDAMENTALS OF NANO ELECTRONICS AND NANO TECHNOLOGY							9
Top-down approach - Bottom-up approach - Scaling to Nano, Particles and waves - Quantum mechanics - Time independent Schrodinger wave equation - Quantum dots - Wires and Well.								
UNIT II	NANO MATERIALS SYNTHESIS							9
Introduction and basic properties of Nanomaterials - Methods to produce nanomaterials, Sol gel method - Applications of Nanomaterials - Synthesis and application of Carbon Nano materials - Carbon Nano cones, and nanowires - Nano composites.								
UNIT III	NANOMATERIALS CHARACTERIZATION							9
Optical microscopy - Scanning electron microscopy - Transmission electron microscopy - atomic force microscopy - Scanning tunnelling microscopy-X-Ray Diffraction.								
UNIT IV	NANO ELECTRONIC SENSORS AND DEVICES							9
Single electron transistors - Carbon nanotube FETs and SETs - Semiconductor nanowire FETs and SETs - Molecular SETs and molecular electronics - Quantum well infrared photo detectors.								
UNIT V	APPLICATIONS OF NANOTECHNOLOGY							9
Verilog HDL modeling, data types, behavioral & structural modeling, FSM synthesis, test benches, combinational/sequential circuit realization.								
ACTIVITIES: 1. Visualization of Quantum Confinement using suitable simulation tools. 2. I-V Characteristics of SETs and CNTFETs using NanoHub Tools. 3. Case study on Nanotechnology-Based COVID-19 Diagnostics and Healthcare Solutions. 4. Review of GATE Questions.								
COURSE OUTCOMES: CO1: Understand the basics and the theoretical foundations of Nano electronics. CO2: Obtain the knowledge of Single Electron Devices and carbon based nano electronic devices. CO3: Understand the use of synthesis methods and describe the properties of Nanomaterials. CO4: Analyze the key performance aspects of Nano electronic devices and its characterization. CO5: Understand the applications of nanotechnology and simulate Nanoelectronic devices.								
TOTAL: 45 PERIODS								
WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%								
TEXTBOOKS: 1. Karl Goser, Jan Dienstuhl and Wolfgang R. Fahrner, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, 2nd Edition, Springer, 2022. 2. T. Pradeep, Nano: The Essentials – Understanding Nanoscience and Nanotechnology, 3rd Edition, McGraw-Hill Education, 2021.								
REFERENCES: 1. V. V. Mitin, V. A. Kochelap and M. A. Strosio, Quantum Heterostructures: Microelectronics and Optoelectronics, 2nd Edition, Cambridge University Press. 2. Edward L. Wolf, Nanophysics and Nanotechnology: An Introduction to Modern Concepts in Nanoscience, 3rd Edition, Wiley-VCH, 2020. 3. Richard Booker and Earl Boyson, Nanotechnology for Dummies, 3rd Edition, Wiley, 2020.								

4. Bharat Bhushan (Ed.), Springer Handbook of Nanotechnology, 4th Edition, Springer, 2017 (Latest Edition).
5. Charles P. Poole Jr. and Frank J. Owens, Introduction to Nanotechnology, 2nd Edition, Wiley India, Latest Reprint.
6. Mark A. Ratner and Daniel Ratner, Nanotechnology: A Gentle Introduction to the Next Big Idea, 2nd Edition, Pearson Education, Latest Reprint.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	1
CO2	3	1	3	3	2
CO3	2	1	3	2	2
CO4	3	2	3	3	3
CO5	3	2	3	3	3
AVG	2.6	1.4	3	2.6	2.2

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26002		CYBER SECURITY FOR ELECTRONICS SYSTEM				L	T	P	C
SDG: 9, 4, 8						3	0	0	3
COURSE OBJECTIVES:									
- Understand the fundamentals of cyber security and security threats in electronic and embedded systems. - Learn cryptographic techniques and secure communication methods for electronic and IoT devices. - Apply network and embedded system security techniques to protect electronic systems. - Analyze cyber security solutions for IoT, industrial, and cyber-physical systems. - Design secure electronic systems using hardware security and trusted computing techniques.									
UNIT I		FUNDAMENTALS OF CYBER SECURITY							9
Introduction to Cyber Security – CIA triad – Threats, vulnerabilities and attacks – Malware, ransomware, spyware, botnets – Risk assessment – Security policies – Cyber kill chain – Cyber security standards – Security governance – Introduction to cyber laws and ethics.									
UNIT II		CRYPTOGRAPHY AND SECURE COMMUNICATION							9
Classical cryptography – Symmetric and asymmetric encryption – AES, DES, RSA, ECC – Hash functions (SHA-2, SHA-3) – Digital signatures – Key management – Public Key Infrastructure (PKI) – SSL/TLS – IPSec – Secure communication protocols for embedded and IoT systems.									
UNIT III		NETWORK AND EMBEDDED SYSTEM SECURITY							9
Network security architecture – Firewalls – Intrusion Detection and Prevention Systems (IDS/IPS) – Virtual Private Networks (VPN) – Wireless security (Wi-Fi, Bluetooth, ZigBee, LoRaWAN) – Secure boot – Trusted Platform Module (TPM) – Embedded firmware security – Secure firmware updates – Hardware root of trust.									
UNIT IV		CYBER SECURITY FOR ELECTRONICS SYSTEMS							9
Security in IoT devices – Industrial Control Systems (ICS) and SCADA security – Automotive cyber security – Medical electronics security – Side-channel attacks – Fault injection attacks – Hardware Trojans – Physical Unclonable Functions (PUFs) – FPGA and SoC security – Supply chain security.									
UNIT V		EMERGING TRENDS IN CYBER SECURITY							9
AI-enabled cyber security – Machine learning for intrusion detection – Blockchain for electronic systems – Zero Trust Architecture – Cloud and Edge security – Post-Quantum Cryptography – Security Operations Center (SOC) – Incident response – Cyber forensics – Case studies in cyber-attacks on electronic infrastructures.									
ACTIVITIES:									
- Compare AES, RSA, ECC, SHA-2, and SHA-3 encryption techniques. - Analyze the security of an IoT, automotive, or industrial electronic system.									

3. Prepare Mini Report on recent trends such as AI in Cyber Security, Blockchain, or Post-Quantum Cryptography.
4. Review of GATE Questions.

COURSE OUTCOMES:

CO1: Explain the fundamentals of cyber security for electronic systems.

CO2: Apply cryptographic techniques and secure communication protocols.

CO3: Analyze security mechanisms for embedded systems and IoT.

CO4: Evaluate hardware security techniques for electronic systems.

CO5: Design secure electronic systems using cyber security principles.

TOTAL: 45 PERIODS

WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%

TEXTBOOKS:

1. William Stallings & Lawrie Brown, Computer Security: Principles and Practice, 5th Edition, Pearson, 2024.
2. William Stallings, Cryptography and Network Security: Principles and Practice, 8th Edition, Pearson, 2023.

REFERENCES:

1. Charles P. Pfleeger, Shari Lawrence Pfleeger & Jonathan Margulies, Security in Computing, 6th Edition, Pearson, 2022.
2. Nina Godbole & Sunit Belapure, Cyber Security: Understanding Cyber Crimes, Computer Forensics and Legal Perspectives, 2nd Edition, Wiley India.
3. Debdeep Mukhopadhyay, Hardware Security: Design, Threats and Safeguards, CRC Press.
4. Douglas Stinson & Maura Paterson, Cryptography: Theory and Practice, 5th Edition, CRC Press.
5. Joseph Migga Kizza, Guide to Computer Network Security, 6th Edition, Springer.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	3	2	-	2	2
CO2	3	3	2	3	2
CO3	3	3	3	3	3
CO4	2	3	3	3	3
CO5	2	3	3	3	3
AVG	2.6	2.8	2.2	2.8	2.6

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


Chairman
Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

AE26003		RF INTEGRATED CIRCUIT DESIGN				L	T	P	C
SDG: 9. 7						3	0	0	3
COURSE OBJECTIVES:									
- Understand the fundamentals of CMOS RF devices, transceiver architectures, and RF performance parameters. - Analyze impedance matching networks and RF amplifier circuits. - Study RF power amplifiers, feedback techniques, and stability analysis. - Understand the operation and design of RF mixers and oscillators. - Analyze PLLs and frequency synthesizers used in RF communication systems.									
UNIT I	CMOS PHYSICS, TRANSCIVER SPECIFICATIONS AND ARCHITECTURES								9
Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two-port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct up conversion Transmitter, Two-step up conversion Transmitter.									
UNIT II	IMPEDANCE MATCHING AND AMPLIFIERS								9
S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.									
UNIT III	FEEDBACK SYSTEMS AND POWER AMPLIFIERS								9
Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.									
UNIT IV	MIXERS AND OSCILLATORS								9
Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.									
UNIT V	PLL AND FREQUENCY SYNTHESIZERS								9
Linearized Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.									
ACTIVITIES:									
- Design and simulate a CMOS Low Noise Amplifier (LNA) and analyze its performance. - Analyze the performance of RF power amplifiers with respect to stability and efficiency. - Compare RF mixers and oscillators based on their performance characteristics. - Review of GATE Questions.									
COURSE OUTCOMES:									
CO1: Explain CMOS RF devices, transceiver architectures, and RF performance parameters.									
CO2: Design impedance matching networks and RF amplifiers.									
CO3: Analyze RF power amplifiers for stability, efficiency, and linearity.									
CO4: Design and evaluate RF mixers and oscillators.									
CO5: Analyze PLL-based frequency synthesizers for RF communication systems.									
TOTAL: 45 PERIODS									
WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%									
TEXTBOOKS:									
- Behzad Razavi, RF Microelectronics, 3rd Edition, Pearson Education, 2023. - Thomas H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, 3rd Edition, Cambridge University Press, 2021.									
REFERENCES:									
- Christopher Bowick, RF Circuit Design, 3rd Edition, Newnes (Elsevier), 2021. - John W. M. Rogers and Calvin Plett, Radio Frequency Integrated Circuit Design, 2nd Edition, Artech House, Latest Reprint.									

3. Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2nd Edition, McGraw-Hill Education, Latest Reprint.
4. B. Razavi (Ed.), Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design, Wiley-IEEE Press, Latest Reprint.
5. Ulrich L. Rohde and David P. Newkirk, RF/Microwave Circuit Design for Wireless Applications, 2nd Edition, Wiley, Latest Reprint.
6. David M. Pozar, Microwave Engineering, 5th Edition, John Wiley & Sons, 2022.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	2
CO2	3	2	3	3	3
CO3	3	2	3	3	2
CO4	3	2	3	3	3
CO5	3	2	3	3	3
AVG	2.8	1.8	3	2.8	2.6

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26004		ELECTROMAGNETIC INTERFERENCE AND				L	T	P	C
SDG: 9, 3, 11		COMPATIBILITY				3	0	0	3
COURSE OBJECTIVES:									
- Understand the fundamentals of Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC). - Analyze EMI sources and coupling mechanisms in electronic systems. - Study EMI control techniques, grounding, shielding, filtering, and EMC standards. - Understand EMI/EMC measurement and testing techniques. - Design EMC-compliant electronic systems and PCB layouts.									
UNIT I		INTRODUCTION TO EMI & EMC							9
Definitions and Concepts – EMC Environment - EMC Testing Categories - Basic Electromagnetic Theory: Maxwell's equations and their application in EMC, Near-field and far-field approximations, Concepts of impedance.									
UNIT II		EMI COUPLING MECHANISMS							9
Coupling Paths - basic coupling mechanisms: Conducted Coupling, Capacitive Coupling, Inductive/Magnetic Coupling, Radiative / Electromagnetic Coupling – Crosstalk - Transient Sources - Automotive transients.									
UNIT III		EMI MITIGATION TECHNIQUES & EMC STANDARDS							9
Shielding – Grounding – Filtering – Cabling – Bonding - Need for Standards - National and International EMC Standardizing Organizations: IEC, FCC, CISPR, ANSI, BSI, CENELEC, ETSI - Key Standards and Specifications: MIL-STD, Electro Magnetic Emission and Susceptibility standards.									
UNIT IV		EMI TEST METHODS AND INSTRUMENTATION							9
Fundamental Considerations - Emission Testing: Conducted Emissions, Radiated Emissions - Immunity/Susceptibility Testing: Conducted Immunity, Radiated Immunity, ESD Testing, Transient Immunity - Test Equipment.									
UNIT V		PCB DESIGN FOR EMC COMPLIANCE							9
PCB Layout and Stack-up - Signal Integrity Considerations - Mixed-Signal PCB Layout: Grounding and power distribution for mixed-signal systems, Isolation of sensitive circuits - Component Placement for EMC.									
ACTIVITIES:									
- Identify and Classify EMI Coupling Mechanisms in Real Devices. - Mini-Report on EMI Mitigation and EMC Standards. - Analyzing PCB Layout for EMC Issues.									



Chairman
Board of Studies
Department of Electronics and Communication Engineering
Engineering College

4. Review of GATE Questions.

COURSE OUTCOMES:

CO1: Explain the fundamentals of EMI and EMC in electronic systems.

CO2: Analyze EMI sources and coupling mechanisms.

CO3: Apply EMI control techniques and EMC standards.

CO4: Evaluate EMI/EMC testing methods and measurement techniques.

CO5: Design EMC-compliant electronic systems and PCB layouts.

TOTAL: 45 PERIODS

WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%

TEXTBOOKS:

1. Henry W. Ott, Electromagnetic Compatibility Engineering, 1st Edition (Latest Reprint), John Wiley & Sons, 2022.
2. David A. Weston, Electromagnetic Compatibility: Principles and Applications, 3rd Edition, CRC Press, 2017 (Latest Reprint).

REFERENCES:

1. Clayton R. Paul, Introduction to Electromagnetic Compatibility, 2nd Edition, John Wiley & Sons, Latest Reprint.
2. Tim Williams, EMC for Product Designers, 5th Edition, Newnes (Elsevier), 2017 (Latest Reprint).
3. Bruce R. Archambeault, James Drewniak and Omar M. Ramahi, EMI/EMC Computational Modeling Handbook, 2nd Edition, Springer, Latest Reprint.
4. Todd H. Hubing, EMC and the Printed Circuit Board: Design, Theory and Layout Made Simple, Latest Edition, Wiley-IEEE Press.
5. Michel Mardiguian, Electromagnetic Interference Troubleshooting and Techniques, Latest Edition, Springer.
6. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Latest Edition, Prentice Hall.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	1
CO2	3	1	3	3	2
CO3	3	2	3	3	2
CO4	3	2	3	2	3
CO5	3	2	3	3	3
AVG	2.8	1.6	3	2.6	2.2

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


Chairman
Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

AE26005	ADVANCED MICROPROCESSORS AND MICROCONTROLLERS ARCHITECTURES		L	T	P	C
SDG: 9, 7, 12			3	0	0	3
COURSE OBJECTIVES:						
- Understand the fundamentals of modern microprocessor architectures and performance techniques. - Study the architecture and operation of Intel 32-bit and Pentium processors. - Analyze 64-bit processor architectures, memory organization, and multicore systems. - Understand ARM processor architecture, instruction sets, and memory organization. - Study the architecture, peripherals, and interfacing of PIC32 microcontrollers.						
UNIT I	MICROPROCESSOR ARCHITECTURE					9
Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.						
UNIT II	32-BIT MICROPROCESSORS					9
Intel 80386 Microprocessor: Architecture - Registers – Descriptors - Real Mode - Protected mode - Virtual 8086 mode - Paging and Segmentation - Comparison with 80486 Microprocessor. Pentium class of processors: RISC and CISC architectures - Superscalar Architecture - MMX technology – SSE – Pipelining - Branch Prediction techniques – FPU - Comparative study of features of Pentium-II, Pentium-III and Pentium-IV processors.						
UNIT III	64 -BIT MICROPROCESSORS					9
Intel 64-bit processors: Overview of 64-bit processor execution environment – Memory organization – IA-32 memory models – Memory organization in 64-bit mode – Extended physical addressing in protected mode - Basic program execution registers – Operand addressing. Multicore Architectures: Concepts – Power reduction techniques in processors – Comparison of Intel Skylake, Goldmont and Ice Lake microarchitectures.						
UNIT IV	HIGH PERFORMANCE RISC ARCHITECTURE					9
Cortex-M Architecture: Introduction to Cortex-M Microcontroller, Microprocessor Architecture, Nested Interrupt Vector Controller, Bus System and Bus Matrix, Memory and Peripherals, Debug Systems, Exceptions and Interrupts Architecture, The ARM64 CPU Architecture, ARM CPU Registers, the Memory Subsystem, ARM- 16/32-bit THUMB instruction set.						
UNIT V	PIC MICROCONTROLLERS					9
The PIC32: Pins, Peripherals, and Special Function Registers, PIC32, The Physical Memory Map, Virtual Memory Map, Configuration Bits, Interrupts, Digital I/O, Counter/Timers, I2C Interfacing –UART, SPI, Flash memory.						
ACTIVITIES:						
- Comparative study of cache hierarchy in modern processors. - Mini-Presentation on Intel 80386 architecture and operating modes - Case study on ARM processors in mobile and IoT devices - Review of GATE Questions.						
COURSE OUTCOMES:						
CO1: Explain the fundamentals of modern microprocessor architectures.						
CO2: Analyze the architecture and operation of Intel 32-bit microprocessors.						
CO3: Evaluate 64-bit processors and multicore architectures.						
CO4: Develop embedded applications using ARM processors.						
CO5: Interface and program PIC32 microcontrollers for embedded applications.						
						TOTAL: 45 PERIODS
WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%						
TEXTBOOKS:						
- Barry B. Brey, The Intel Microprocessors: Architecture, Programming, and Interfacing, 9th Edition, Pearson Education, 2024. - Joseph Yiu, The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors, 3rd Edition, Newnes (Elsevier), 2020.						

REFERENCES:

1. William Stallings, Computer Organization and Architecture: Designing for Performance, 11th Edition, Pearson Education, 2022.
2. David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface (ARM Edition), 2nd Edition, Morgan Kaufmann (Elsevier), 2021.
3. Joseph Yiu, The Definitive Guide to ARM® Cortex®-M23 and Cortex®-M33 Processors, 1st Edition, Newnes (Elsevier), 2020.
4. Lucio Di Jasio, Programming 32-bit Microcontrollers in C: Exploring the PIC32, 2nd Edition, Newnes (Elsevier), Latest Reprint.
5. Muhammad Ali Mazidi, Sarmad Naimi and Sepehr Naimi, ARM Assembly Language Programming and Architecture, Latest Edition, Pearson Education.
6. Andrew N. Sloss, Dominic Symes and Chris Wright, ARM System Developer's Guide: Designing and Optimizing System Software, Morgan Kaufmann, Latest Reprint.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	1
CO2	3	1	3	2	2
CO3	3	1	3	2	2
CO4	3	2	3	3	3
CO5	3	2	2	3	3
AVG	2.8	1.4	2.8	2.4	2.2

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26006	ADVANCED COMPUTER ARCHITECTURE DESIGN			
SDG: 9, 7, 13	L	T	P	C
	3	0	0	3
COURSE OBJECTIVES:				
- Understand the fundamentals of parallel computing and computer architectures. - Study program partitioning, scheduling, and performance evaluation in parallel systems. - Analyze processor architecture, memory hierarchy, and cache coherence techniques. - Understand pipelined, superscalar, and multiprocessor architectures. - Explore vector processing, multithreading, and parallel programming concepts.				
UNIT I	THEORY OF PARALLELISM			
Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.				9
UNIT II	PARTITIONING AND SCHEDULING			
Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance - performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.				9
UNIT III	HARDWARE TECHNOLOGIES			
Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory – Bus Arbitration, cache memory organizations, shared memory organizations, sequential and weak consistency models.				9
UNIT IV	PIPELINING, SUPERSCALAR, PARALLEL AND SCALABLE ARCHITECTURE			
Linear and Non-Linear Pipeline processor – Instruction and Arithmetic Pipeline Design – Superscalar and Super pipeline Design – Multiprocessor Interconnects – Cache Coherence and Synchronization mechanism – Message Passing Mechanism – Flow Control Strategies – Multicast Routing Strategies.				9

UNIT V	MULTIVECTOR AND SIMD COMPUTERS	9
Vector processing Principles – Compound Vector Processing – SIMD Computer Organisation – Synchronized MIMD machine – Latency Hiding Technique – Multithreading – Scalable and Multithreaded Architectures – Data Flow and Hybrid Architectures - Parallel models, Languages and compilers, Parallel program development and environments.		
ACTIVITIES:		
1. Comparative study of PRAM vs SIMD vs MIMD architectures. 2. Mini-Report on Cache Coherence Protocols. 3. Mini-Presentation on Task Scheduling Techniques in Multicore Systems. 4. Review of GATE Questions.		
COURSE OUTCOMES:		
CO1: Explain the fundamentals of parallel computer architectures.		
CO2: Analyze partitioning, scheduling, and performance of parallel systems.		
CO3: Evaluate processor architectures, memory hierarchy, and cache coherence.		
CO4: Analyze pipelined, superscalar, and multiprocessor architectures.		
CO5: Apply parallel processing and programming techniques to solve computational problems.		
TOTAL: 45 PERIODS		
WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%		
TEXTBOOKS:		
1. Kai Hwang, Advanced Computer Architecture: Parallelism, Scalability, Programmability, 2nd Edition, McGraw-Hill Education, Latest Reprint. 2. John L. Hennessy and David A. Patterson, Computer Architecture: A Quantitative Approach, 6th Edition, Morgan Kaufmann (Elsevier), 2019.		
REFERENCES:		
1. David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface (ARM Edition), 2nd Edition, Morgan Kaufmann (Elsevier), 2021. 2. William Stallings, Computer Organization and Architecture: Designing for Performance, 11th Edition, Pearson Education, 2022. 3. Michael J. Flynn and Wayne Luk, Computer System Design: System-on-Chip, Wiley, Latest Edition. 4. Kai Hwang and Naresh Jotwani, Advanced Computer Architecture: Parallelism, Scalability, Programmability, McGraw-Hill Education, Latest Reprint. 5. Barry Wilkinson and Michael Allen, Parallel Programming: Techniques and Applications Using Networked Workstations and Parallel Computers, 2nd Edition, Pearson Education. 6. Michael Quinn, Parallel Programming in C with MPI and OpenMP, McGraw-Hill Education, Latest Reprint.		

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	1
CO2	3	1	3	2	2
CO3	3	1	3	2	2
CO4	3	2	3	3	3
CO5	3	2	2	3	3
AVG	2.8	1.4	2.8	2.4	2.2

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


 Chairman
 Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

AE26007		SIGNAL INTEGRITY FOR HIGH-SPEED DESIGN				L	T	P	C
SDG: 9, 11, 12						3	0	0	3
COURSE OBJECTIVES:									
- Understand the fundamentals of signal integrity in high-speed electronic systems. - Analyze transmission line effects, reflections, and termination techniques. - Study crosstalk and noise reduction techniques in PCB interconnects. - Understand differential signaling and impedance control for high-speed circuits. - Analyze clock distribution and timing issues in digital systems.									
UNIT I		INTRODUCTION TO SIGNAL INTEGRITY							9
Introduction to Signal Integrity – Signal quality in high-speed digital systems – Crosstalk – Ground bounce – Power integrity and rail collapse noise – Electromagnetic Interference (EMI) – Controlled impedance – Resistance, capacitance and inductance in PCB interconnects – Power and ground planes – Decoupling capacitors – Self and mutual inductance – Return current paths – Signal integrity issues in high-speed PCB design.									
UNIT II		TRANSMISSION LINES AND REFLECTIONS							9
Transmission line fundamentals – Characteristic impedance – Controlled impedance – Signal propagation and return paths – Signal reflections – Source and load termination techniques – Bounce diagrams – Reflections due to capacitive and inductive discontinuities – Effects of vias and PCB discontinuities – Transmission line losses – Skin effect – Dielectric losses – Signal integrity design guidelines.									
UNIT III		CROSSTALK							9
Coupling: Capacitance and Inductance, Cross Talk in Transmission Lines, Cross Talk in Uniform Transmission Lines and Saturation Length, Capacitively Coupled Currents, Inductively Coupled Currents, Near-End Cross Talk, Far-End Cross Talk, Decreasing Far-End Cross Talk, Guard Traces, Cross Talk and Dielectric, Cross Talk and Timing, Switching Noise.									
UNIT IV		DIFFERENTIAL SIGNALING							9
Differential Signaling, A Differential Pair, Differential Impedance with No Coupling, The Impact from Coupling, Calculating Differential Impedance, The Return-Current Distribution in a Differential Pair, Ideal Coupled Transmission-Line Model or an Ideal Differential Pair, Cross Talk in Differential Pairs, Crossing a Gap in the Return Path.									
UNIT V		CLOCK DISTRIBUTION AND CLOCK OSCILLATORS							9
Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.									
ACTIVITIES:									
Poster: Explain impedance, ground bounce, and EMI. Quiz: Identify near-end and far-end crosstalk using simple diagrams. Simulation: Analyze differential pairs using an EDA tool. - Review of GATE Questions.									
COURSE OUTCOMES:									
CO1: Explain the fundamentals of signal integrity in high-speed systems.									
CO2: Analyze transmission lines and signal reflections.									
CO3: Evaluate crosstalk and noise in PCB interconnects.									
CO4: Analyze differential signaling and impedance matching.									
CO5: Design reliable clock distribution networks for high-speed circuits.									
								TOTAL: 45 PERIODS	
WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%									
TEXTBOOKS:									
- Eric Bogatin, Signal and Power Integrity – Simplified, 4th Edition, Pearson Education, 2022. - Stephen H. Hall, Howard L. Heck and James A. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, 2nd Edition, Wiley-IEEE Press, Latest Reprint.									

REFERENCES:

1. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, 1st Edition, Prentice Hall, Latest Reprint.
2. Howard Johnson and Martin Graham, High-Speed Digital Design: A Handbook of Black Magic, 1st Edition, Pearson Education, Latest Reprint.
3. Howard Johnson, High-Speed Signal Propagation: Advanced Black Magic, Prentice Hall, Latest Reprint.
4. Brian C. Wadell, Transmission Line Design Handbook, Artech House, Latest Reprint.
5. Ritchey Lee W. and John Zasio, Right the First Time: A Practical Handbook on High-Speed PCB and System Design, 2nd Edition, Speeding Edge, Latest Reprint.
6. Stephen C. Thierauf, High-Speed Circuit Board Signal Integrity, Artech House, Latest Reprint.

CO's-PO's & PSO's MAPPING

COs	PO1	PO2	PO3	PSO1	PSO2
CO1	3	2	—	3	2
CO2	3	3	2	3	2
CO3	3	3	2	3	3
CO4	2	3	3	3	3
CO5	2	3	3	3	3
AVG	2.6	2.8	2.0	3	2.6

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26008	VLSI INTERCONNECTS				L	T	P	C
SDG: 9, 7					3	0	0	3

COURSE OBJECTIVES:

- Understand the basics, trends, and challenges of VLSI interconnects.
- Study the electrical characteristics and modeling of VLSI interconnects.
- Understand crosstalk, noise, and delay effects in high-speed interconnects.
- Learn about electromigration, reliability issues, and interconnect failures.
- Explore emerging interconnect technologies for future nanoscale VLSI systems.

UNIT I	INTRODUCTION TO VLSI INTERCONNECTS	9
Types of interconnects – Interconnect trends – Coupling capacitance – Inductive effects – Interconnect metrics – Signal transmission on interconnects – On-chip interconnections – Package-level interconnections – Design methodologies for interconnects – Stress void and electromigration phenomenon – Interconnections for VLSI applications – Copper interconnections – Fabrication and Damascene processing – Scaling of interconnects.		
UNIT II	INTERCONNECT MODELING	9
Lossless and lossy transmission line models – Optimum line model selection – Circuit models of interconnects – Ideal, capacitive and resistive interconnects – Resistive interconnect trees – Scaling effects on interconnect delay – Cross-capacitances and Miller effect – Interconnect power consumption.		
UNIT III	CROSSTALK IN INTERCONNECTS	9
Definition of crosstalk – Mutual inductance and mutual capacitance – Inductance and capacitance matrix – Crosstalk-induced noise – Simulation using equivalent circuit models – Minimization of crosstalk – Crosstalk-induced delay – Energy dissipation due to crosstalk – Crosstalk effects in logic VLSI circuits.		
UNIT IV	NOISE DETECTION, AVOIDANCE AND ELECTROMIGRATION ANALYSIS	9
Crosstalk avoidance – Switching noise avoidance – Noise detection problem – Crosstalk-induced spurious signal detection – IDDx test approaches for crosstalk detection – Electromigration in VLSI metallizations – Modeling of electromigration due to repetitive pulsed currents – Electromigration in copper interconnections – Failure analysis of VLSI interconnection components – Computer-aided failure analysis.		
UNIT V	FUTURE INTERCONNECTION TECHNOLOGIES	9


 Chairman
 Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

Demands in future interconnects – Optical interconnections – Superconducting interconnects – Silicon nanowires – Metallic interconnections – Carbon nanotube interconnections – Quantum-cell-based wireless interconnections – Emerging nanoscale interconnect technologies.

ACTIVITIES:

1. Model RC and RLC interconnect modeling using EDA tools.
2. Model capacitive and inductive coupling effects using EDA tools.
3. Mini-Report on Reliability issues in VLSI interconnect networks.
4. Review of GATE Questions.

COURSE OUTCOMES:

- CO1:** Explain the fundamentals, fabrication, and scaling of VLSI interconnects.
CO2: Analyze the electrical characteristics and models of VLSI interconnects.
CO3: Explain crosstalk, signal integrity, and delay in high-speed interconnects.
CO4: Analyze reliability issues and electromigration effects in VLSI interconnects.
CO5: Describe emerging interconnect technologies for future VLSI systems.

TOTAL: 45 PERIODS

WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%

TEXTBOOKS:

1. Ashok K. Goel, High-Speed VLSI Interconnections: Modeling, Analysis, and Simulation, 2nd Edition, Wiley-IEEE Press, 2007.
2. K. C. Saraswat and F. Mohammadi, Interconnect Technology and Design for Gigascale Integration, Springer, Latest Edition.
3. J. A. Davis and J. D. Meindl, Interconnect Technology and Design for Gigascale Integration, Springer, Latest Edition.

REFERENCES:

1. W. J. Dally and J. W. Poulton, Digital Systems Engineering, Cambridge University Press, Latest Edition.
2. Howard Johnson and Martin Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, Latest Edition.
3. H. B. Bakoglu, Circuits, Interconnections, and Packaging for VLSI, Addison-Wesley, Latest Edition.
4. Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 4th Edition, McGraw Hill Education, 2014.
5. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolić, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education, 2003.
6. J. D. Meindl, Interconnect Technology and Design for Gigascale Integration, Springer, Latest Edition.
7. Madhavan Swaminathan and A. Ege Engin, Power Integrity Modeling and Design for Semiconductors and Systems, Prentice Hall, Latest Edition.
8. Stephen H. Hall, Garrett W. Hall and James A. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-IEEE Press, Latest Edition.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	1	1	3	2	1
CO2	3	1	3	3	3
CO3	2	1	3	3	2
CO4	3	1	3	2	3
CO5	2	2	3	3	3
AVG	2.2	1.2	3	2.6	2.4

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


Chairman
Board of Studies
Department of Electronics and Communication Engineering
Kingston Engineering College
Vellore - 632 059

AE26009	SEMICONDUCTOR MEMORY DESIGN	L	T	P	C
SDG: 9, 4		3	0	0	3
COURSE OBJECTIVES:					
- Understand the architecture and operation of SRAM and DRAM memory systems. - Study non-volatile memory technologies and their applications. - Analyze memory faults, testing methods, and design-for-testability techniques. - Evaluate memory reliability, radiation effects, and fault-tolerant designs. - Explore advanced memory technologies and future memory architectures.					
UNIT I	RANDOM ACCESS MEMORY TECHNOLOGIES				9
Static Random-Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation - Silicon on Insulator (SOI) Technology- SRAM Architectures and Technologies-Application Specific SRAMs. Dynamic Random-Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures - Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.					
UNIT II	NONVOLATILE MEMORIES				9
Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology and Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.					
UNIT III	MEMORY FAULT MODELING & TESTING				9
RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing- Application Specific Memory Testing.					
UNIT IV	RELIABILITY AND RADIATION EFFECTS				9
General Reliability Issues-RAM Failure Modes and Mechanism-Design for Reliability- Reliability Test Structures-Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques- Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics.					
UNIT V	ADVANCE D MEMORIES AND PACKAGING TECHNOLOGIES				9
Ferroelectric Random-Access Memories (FRAMs)-Gallium Arsenide (GaAs)FRAMs-Analog Memories-Magneto resistive. Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues- Memory Cards-High Density Memory Packaging Future Directions.					
ACTIVITIES:					
- Simulate SRAM and DRAM cell structures using EDA tools. - Quiz or Task where students identify and classify memory fault types and appropriate test methods. - Prepare a technical poster/report on radiation effects and hardening techniques used in memory design. - Review of GATE Questions.					
COURSE OUTCOMES:					
CO1: Analyze the architecture and operation of SRAM and DRAM memory systems.					
CO2: Evaluate non-volatile memory technologies and their applications.					
CO3: Apply memory testing and design-for-testability (DFT) techniques.					
CO4: Analyze memory reliability and fault-tolerant design techniques.					
CO5: Investigate advanced memory technologies and future memory architectures.					
TOTAL: 45 PERIODS					
WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%					
TEXTBOOKS:					
- Ashok K. Sharma, Semiconductor Memories: Technology, Testing, and Reliability, Wiley-IEEE Press, Latest Edition. - Betty Prince, Semiconductor Memories: A Handbook of Design, Manufacture and Application, 2nd Edition, John Wiley & Sons, Latest Edition.					

3. Kiyoo Itoh, VLSI Memory Chip Design. Springer, Latest Edition.

REFERENCES:

1. Betty Prince, High Performance Memories: New Architecture DRAMs and SRAMs—Evolution and Function, John Wiley & Sons, Latest Edition.
2. Ashok K. Sharma, Advanced Semiconductor Memories: Architectures, Designs, and Applications, Wiley-IEEE Press, Latest Edition.
3. Kiyoo Itoh, VLSI Memory Chip Design, Springer, Latest Edition.
4. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, 4th Edition, Wiley-IEEE Press, 2019.
5. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolić, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education, Latest Edition.
6. Neil H. E. Weste and David Money Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th Edition, Pearson Education, Latest Edition.
7. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, VLSI Test Principles and Architectures: Design for Testability, Morgan Kaufmann, Latest Edition.
8. M. L. Bushnell and Vishwani D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer, Latest Edition.
9. R. Rajsuman, System-on-a-Chip: Design and Test, Artech House, Latest Edition.
10. Takayuki Kawahara and Hiroyuki Mizuno, Green Computing with Emerging Memory: Low-Power Computation for Social Innovation, Springer, Latest Edition.
11. Yuan Xie, J. Cong and S. S. Sapatnekar, Three-Dimensional Integrated Circuit Design: EDA, Design and Microarchitectures, Springer, Latest Edition.
12. Mohammad Tehranipoor and Cliff Wang, Introduction to Hardware Security and Trust, Springer, Latest Edition.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	3	2
CO2	2	1	3	3	2
CO3	3	1	3	2	3
CO4	3	1	3	2	3
CO5	3	2	3	3	3
AVG	2.6	1.2	3	2.6	2.6

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


Chairman
Board of Studies
Department of Electronics and Communication Engineering
Kingston Engineering College
Vellore - 632 059

AE26010	ALGORITHMS FOR VLSI PHYSICAL DESIGN AUTOMATION	L	T	P	C
SDG: 9, 8		3	0	0	3

COURSE OBJECTIVES:

- Understand the basics of VLSI design flow and EDA tools.
- Learn graph theory, data structures, and optimization techniques used in VLSI design.
- Study partitioning, placement, and layout compaction methods.
- Understand floor planning and routing techniques in VLSI physical design.
- Learn modeling, simulation, and logic synthesis for VLSI design automation.

UNIT I INTRODUCTION TO VLSI DESIGN AUTOMATION

9

Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles – Review of VLSI Design Automation Tools.

UNIT II DATA STRUCTURES AND BASIC ALGORITHMS

9

Basic Data Structures, Graph Algorithms: Graph Search Algorithms, Spanning Tree Algorithms, Shortest Path Algorithms, Classes of Graphs in Physical Design, Relationship Between Graph Classes, Graph Problems in Physical Design, Algorithms for Interval Graphs, Algorithms for Permutation Graphs, Algorithms for Circle Graphs.

UNIT III ALGORITHMS FOR LAYOUT COMPACTION, PLACEMENT AND PARTITIONING

9

Layout Compaction: Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint Graph Compaction – Placement and Partitioning: Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithms, Partitioning: The Kernighan-Lin Partitioning Algorithm.

UNIT IV ALGORITHMS FOR FLOOR PLANNING AND ROUTING

9

Floor planning: Floor planning Concepts, Terminology and Floorplan Representation, Optimization Problems in Floor planning, Shape Functions and Floorplan Sizing. Routing: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing.

UNIT V MODELLING AND SIMULATION AND SYNTHESIS

9

Simulation: Gate Level Modeling and Simulation, Switch-level Modeling and Simulation – Logic Synthesis and Verification: Combinational Logic Synthesis, Binary Decision Diagrams, Two-level Logic Synthesis, High level Synthesis.

ACTIVITIES:

1. Analyze graph representation of circuit layouts using EDA tools.
2. Implement Kernighan-Lin partitioning algorithm using any appropriate simulation tools.
3. Congestion analysis and routing optimization using EDA tools
4. Logic synthesis using EDA tools.
5. Review of GATE Questions.

COURSE OUTCOMES:

CO1: Explain VLSI design flow and EDA tools.

CO2: Apply graph theory and optimization techniques in VLSI physical design.

CO3: Analyze partitioning, placement, and layout compaction techniques.

CO4: Design floor planning and routing for VLSI circuits.

CO5: Apply modeling, simulation, and logic synthesis using EDA tools.

WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60% **TOTAL: 45 PERIODS**

TEXTBOOKS:

1. Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Springer, 1999.
2. S. H. Gerez, Algorithms for VLSI Design Automation, John Wiley & Sons, Latest Edition.
- Sabih H. Gerez, Algorithms for VLSI Design Automation, John Wiley & Sons, 1999.

REFERENCES:

1. Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer, Latest Edition.
2. Andrew B. Kahng, Jens Lienig, Igor L. Markov and Jin Hu, VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer, Latest Edition.

3. Sadiq M. Sait and Habib Youssef, VLSI Physical Design Automation: Theory and Practice, World Scientific, Latest Edition.
4. Giovanni De Micheli, Synthesis and Optimization of Digital Circuits, McGraw-Hill, Latest Edition.
5. J. Bhasker, A VHDL Primer, 3rd Edition, Pearson Education, Latest Edition.
6. M. J. S. Smith, Application-Specific Integrated Circuits, Pearson Education, Latest Edition.
7. Wayne Wolf, Modern VLSI Design: IP-Based Design, 4th Edition, Pearson Education, Latest Edition.
8. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolić, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education, Latest Edition.
9. Neil H. E. Weste and David Money Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th Edition, Pearson Education, Latest Edition.
10. Laung-Terng Wang, Yao-Wen Chang and Kwang-Ting Cheng, Electronic Design Automation: Synthesis, Verification, and Test, Morgan Kaufmann, Latest Edition.
11. Charles J. Alpert, Dinesh P. Mehta and Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, Latest Edition.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	1	1	3	2	1
CO2	3	1	3	3	2
CO3	3	1	3	3	3
CO4	3	1	3	3	3
CO5	3	2	3	3	3
AVG	2.6	1.2	3	2.8	2.4

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


 Chairman
 Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

AE26011	STATISTICAL ANALYSIS AND OPTIMIZATION FOR VLSI				L	T	P	C
SDG: 9, 12					3	0	0	3
COURSE OBJECTIVES:								
- Understand process variations and their effects on VLSI circuit performance and yield. - Study statistical models for performance and variability analysis. - Analyze statistical timing techniques for VLSI circuits. - Evaluate statistical power and yield analysis methods. - Apply statistical optimization techniques to improve VLSI circuit performance and manufacturability.								
UNIT I	INTRODUCTION TO PROCESS VARIATIONS							9
Sources of Variations: Process, Environmental, Modeling and other Sources of Variations, Components of Variation: Inter-die Variations, Intra-die variations, Impact on Performance.								
UNIT II	DATA STRUCTURES AND BASIC ALGORITHMS							9
Monte Carlo Techniques: Sampling Probability Distributions using Acceptance-Rejection Method and Multivariate Gaussian random variables, Process Variation Modeling: Pelgrom's Model, Principal Components Based Modeling, Quad-Tree Based Modeling, Electromigration Modeling, Performance Modeling: Response Surface Methodology, Delay Modeling, Interconnect Delay Models: Statistical Delay Metrics.								
UNIT III	STATISTICAL TIMING ANALYSIS							9
Introduction, Block-Based Timing Analysis, Discretized Delay PDFs, Reconvergent Fanouts, Canonical Delay PDFs, Multiple Input Switching, Path-Based Timing Analysis, Parameter-Space Techniques, Bayesian Networks.								
UNIT IV	STATISTICAL POWER AND YIELD ANALYSIS							9
Power Analysis: Leakage Models, High-Level Statistical Analysis, Gate-Level Statistical Analysis, Dynamic Power, Leakage Power: Estimating Parameters of the Distribution, Estimating the probability density function, Temperature and Power Supply Variations, Yield Analysis: High-Level Yield Estimation, Gate-Level Yield Estimation: Timing Analysis, Leakage Power Analysis, Yield Estimation, Supply Voltage Sensitivity.								
UNIT V	STATISTICAL OPTIMIZATION TECHNIQUES							9
Optimization of Process Parameters, Gate Sizing, Buffer Insertion, Threshold Voltage Assignment.								
ACTIVITIES:								
- Analyze variation effects on device parameters using appropriate simulation tools. - Monte Carlo analysis of circuit parameters using appropriate simulation tools. - Probability density function-based delay analysis using appropriate simulation tools. - Leakage power variation under process corners using EDA tools. - Gate sizing and threshold voltage optimization using appropriate simulation tools - Review of GATE Questions.								
COURSE OUTCOMES:								
CO1: Analyze the effects of variations on VLSI circuit performance.								
CO2: Apply statistical modeling techniques for VLSI performance analysis.								
CO3: Perform statistical timing analysis for VLSI circuits.								
CO4: Analyze power consumption and yield in VLSI circuits.								
CO5: Apply statistical optimization techniques to improve VLSI circuit performance and yield.								
TOTAL: 45 PERIODS								
WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%								
TEXTBOOKS:								
- Sani R. Nassif, David J. Allstot and Farid N. Najm, Statistical Analysis and Optimization for VLSI: Timing and Power, Springer, Latest Edition/Reprint. - Ashish Srivastava, Dennis Sylvester and David Blaauw, Statistical Analysis and Optimization for VLSI: Timing and Power, Springer, Latest Edition/Reprint								
REFERENCES:								

1. Duane S. Boning and Srivatsan S. Chakravarthi, Variation-Aware Design of Custom Integrated Circuits: A Hands-on Field Guide, Springer, Latest Edition/Reprint.
2. Mohab Anis, Statistical Design of Integrated Circuits, Springer, Latest Edition/Reprint.
3. Khaled Salah, A. H. A. El-Moursy and A. S. El-Rouby, Statistical Design of Integrated Circuits, Springer, Latest Edition/Reprint.
4. Michael Orshansky, Sani Nassif and Duane Boning, Design for Manufacturability and Statistical Design: A Constructive Approach, Springer, Latest Edition/Reprint.
5. David Blaauw, Kaviraj Chopra, Ashish Srivastava and Louis Scheffer, Statistical Timing Analysis: From Basic Principles to State of the Art, IEEE Transactions on Computer-Aided Design, Latest Reprint.
6. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolić, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education, Latest Reprint.
7. Neil H. E. Weste and David Money Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th Edition, Pearson Education, Latest Reprint.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	2
CO2	3	1	3	3	3
CO3	3	1	3	3	2
CO4	2	1	3	3	2
CO5	3	2	3	3	3
AVG	2.6	1.2	3	2.8	2.4

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26012	SYSTEM ON CHIP DESIGN				L	T	P	C
SDG: 9, 11					3	0	0	3
COURSE OBJECTIVES:								
• Understand the architecture and design of modern computer systems. • Analyze processor organization, pipelining, and memory hierarchy. • Study SoC architectures, interconnection networks, and FPGA-based systems. • Understand hardware–software co-design and performance optimization techniques. • Design and evaluate advanced architectures for embedded and high-performance applications.								
UNIT I	SYSTEM ARCHITECTURE: OVERVIEW							9
Components of the system – Processor architectures – Memory and addressing – System-level interconnection – SoC design requirements and specifications – Design integration – Design complexity – Cycle time, die area and cost – Ideal and practical scaling – Area-time-power tradeoff in processor design – Configurability.								
UNIT II	PROCESSOR SELECTION FOR SOC							9
Overview – Soft processors, processor core selection – Instruction set, branches, interrupts and exceptions – Basic elements in instruction handling – Minimizing pipeline delays – Reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors.								
UNIT III	MEMORY DESIGN							9
SoC external memory, SoC internal memory – Scratchpads and cache memory – Cache organization and write policies – Line replacement strategies – Split I/D-caches – Multilevel caches – SoC memory systems – Board-based memory systems – Processor/memory interaction.								
UNIT IV	INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION							9
Bus architectures – SoC standard buses (AMBA, Core Connect) – Processor customization approaches – Reconfigurable technologies – Mapping designs onto reconfigurable devices – FPGA-based design – Architecture of FPGA – FPGA interconnect technology – FPGA memory – Floor planning and routing.								
UNIT V	FPGA-BASED EMBEDDED PROCESSOR							9
Hardware/software task partitioning – FPGA fabric-immersed processors – Soft processors and hard processors – Tool flow for hardware/software co-design – Interfacing processor with memory and								

peripherals – On-chip interfaces: Wishbone, Avalon, OPB – Customized microcontroller design – FPGA-based signal interfacing and conditioning.

ACTIVITIES:

1. Comparative Study on Apple M-Series vs ARM Cortex SoCs.
2. Comparative Study on Intel Core vs AMD Ryzen architectures.
3. Mini Project on FPGA-based embedded controller.
4. Review of GATE Questions.

COURSE OUTCOMES:

CO1: Explain modern computer architectures and processor organization.

CO2: Analyze advanced processor architectures and multicore systems.

CO3: Evaluate memory hierarchy and cache architectures.

CO4: Analyze SoC architectures, interconnection networks, and FPGA platforms.

CO5: Apply FPGA design and hardware–software co-design techniques for embedded systems.

TOTAL: 45 PERIODS

WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%

TEXTBOOKS:

1. Michael J. Flynn and Wayne Luk, Computer System Design: System-on-Chip, John Wiley & Sons, Latest Edition/Reprint.
2. Patrick R. Schaumont, A Practical Introduction to Hardware/Software Codesign, 2nd Edition, Springer, 2013, Latest Reprint.

REFERENCES:

1. David A. Patterson and John L. Hennessy, Computer Organization and Design RISC-V Edition: The Hardware/Software Interface, 2nd Edition, Morgan Kaufmann, 2021.
2. John L. Hennessy and David A. Patterson, Computer Architecture: A Quantitative Approach, 7th Edition, Morgan Kaufmann, 2025.
3. Wayne Wolf, Modern VLSI Design: IP-Based Design, 4th Edition, Pearson Education, Latest Reprint.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	1
CO2	3	1	3	2	2
CO3	3	1	3	2	2
CO4	3	2	3	3	3
CO5	3	2	3	3	3
AVG	2.8	1.4	3	2.4	2.2

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


 Chairman
 Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

AE26013	HARDWARE / SOFTWARE CO-DESIGN				L	T	P	C
SDG: 9, 7					3	0	0	3
COURSE OBJECTIVES:								
- Understand embedded system design and hardware–software co-design concepts. - Study system modeling, partitioning, and synthesis techniques. - Analyze hardware–software partitioning and optimization methods. - Understand prototyping, emulation, and verification techniques. - Design and implement heterogeneous embedded systems using co-design methods.								
UNIT I	SYSTEM SPECIFICATION AND MODELLING							9
Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification And Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor Architectures with One ASIC, Single-Processor Architectures with Many ASICs, Multi-Processor Architectures, Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification.								
UNIT II	HARDWARE/SOFTWARE PARTITIONING							9
The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based on Heuristic Scheduling, HW/SW Partitioning Based on Genetic Algorithms.								
UNIT III	HARDWARE/SOFTWARE CO-SYNTHESIS							9
The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis – Hardware/software co-synthesis algorithms: hardware – software partitioning, distributed system co-synthesis.								
UNIT IV	PROTOTYPING AND EMULATION							9
Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.								
UNIT V	DESIGN SPECIFICATION AND VERIFICATION							9
Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design: System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-Simulation.								
ACTIVITIES:								
- Mini-Presentation on Co-Synthesis Methodologies. - Mini-Report on Distributed embedded system design. - Case Study: FPGA-based autonomous vehicle controller. - Review of GATE Questions.								
COURSE OUTCOMES:								
CO1: Explain embedded system architectures and hardware–software co-design concepts.								
CO2: Apply hardware–software partitioning techniques for embedded system design.								
CO3: Analyze hardware–software co-synthesis techniques for embedded systems.								
CO4: Develop embedded system prototypes using modern platforms.								
CO5: Apply system modeling, verification, and validation techniques for reliable embedded systems.								
TOTAL: 45 PERIODS								
WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%								
ASSESSMENT METHODOLOGY: Quiz (10%), Assignments/Activities (40%), Flipped class (10%), Internal Examinations (40%)								
TEXTBOOKS:								
- Jørgen Staunstrup and Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice", Springer Science & Business Media, 2012. - Patrick R. Schaumont. "A Practical Introduction to Hardware/Software Codesign", Springer, 2010.								

REFERENCES:

1. Frank Vahid and Tony Givargis, "Embedded System Design: A Unified Hardware/Software Introduction", Wiley, 2006.
2. Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", 3rd Edition, Morgan Kaufmann, 2012.
3. Rajesh Gupta, Giovanni De Micheli and Grant Martin, "Hardware/Software Co-Design", Kluwer Academic Publishers.
4. Daniel D. Gajski, Frank Vahid, Sanjiv Narayan and Jie Gong, "Specification and Design of Embedded Systems", Prentice Hall.
5. Peter Marwedel, "Embedded System Design", Springer, 2011.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	1
CO2	3	1	3	3	2
CO3	3	2	3	3	3
CO4	3	2	3	3	3
CO5	3	3	3	3	3
AVG	2.8	1.8	3	2.8	2.4

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26014	MEMS & NEMS				L	T	P	C
SDG: 9, 3					3	0	0	3
COURSE OBJECTIVES:								
- Understand the fundamentals, operating principles, and fabrication processes of MEMS. - Study photolithography, photoresist materials, and pattern transfer techniques. - Understand the fundamentals and fabrication methods of NEMS. - Explore carbon-based materials and fabrication challenges in NEMS. - Study the applications of MEMS and NEMS in various fields.								
UNIT I	FUNDAMENTALS OF MEMS							9
MEMS Introduction - Low Cost - Redundancy and Disposability – Scaling – Made – Substrates –Processing – Mask – Developing – Etching - Road Map and Perspective Silicon Substrate – Silicon Growth – Crystal - Miller Indices – Semiconductor – Doping - Additive Techniques.								
UNIT II	PATTERN TRANSFORMATION OF MEMS							9
Photolithographic Process - Clean room - Photo Resist - Positive Resist - Negative Resist –Working with Resist – Applying Photo Resist - Exposure and Pattern Transfer - Printing Methods – Contact Proximity – Projection Printing - Development and Post Treatment -Masks – Resolution –Sensitivity and Resist Profiles – Mask Alignment - Permanent Resists.								
UNIT III	INTRODUCTION OF NEMS							9
Introduction – Basic properties - Benefits of Nanomachines – Miniaturization - NEMS Memory – Importance of AFM - Top-Down Approach - NEMS devices - NEMS Advantages.								
UNIT IV	NEMS MATERIALS AND FABRICATION							9
Materials – Carbon Allotropes - Carbon Based Materials - Metallic Carbon Nanotubes –Difficulties – Simulations - Current Challenges and future of NEMS – Deposition processes – Lithography – Etching processes.								
UNIT V	MEMS/NEMS DEVICES AND APPLICATIONS							9
Pressure sensor - Piezoresistive sensor - Capacitive sensor – RF applications –Gyroscope – Optical MEMS - Optical Data - Switching - RF MEMS - MEMS switches - MEMS Resonators. Case study: Cantilever piezoelectric actuator, Capacitive accelerometer, Piezoresistive pressure sensor								
ACTIVITIES:								
1. Hands-on session on Silicon wafer orientation and doping simulation using open tools.								

2. Lithography and mask alignment procedure demonstration using open tools.
3. Simulate NEMS memory modeling using nano-electronics simulator.
4. Group Project: Design and simulate a carbon nanotube-based NEMS device
5. Review of GATE Questions.

COURSE OUTCOMES:

CO1: Explain the fundamentals and fabrication processes of MEMS and NEMS.

CO2: Analyze lithography and microfabrication techniques for MEMS/NEMS devices.

CO3: Evaluate MEMS/NEMS devices and nanomaterials for various applications.

CO4: Design MEMS/NEMS-based sensors and actuators.

CO5: Apply emerging MEMS/NEMS technologies in sensing, biomedical, RF, and nanoelectronic applications.

TOTAL: 45 PERIODS

WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%

ASSESSMENT METHODOLOGY: Quiz (10%), Assignments/Activities (40%), Flipped class (10%), Internal Examinations (40%)

TEXTBOOKS:

1. Marc J. Madou, Fundamentals of Microfabrication and Nanotechnology, 3rd Edition, CRC Press, 2011.
2. Tai-Ran Hsu, MEMS and Microsystems: Design, Manufacture, and Nanoscale Engineering, 2nd Edition, John Wiley & Sons, 2008.
3. Minhang Bao, Analysis and Design Principles of MEMS Devices, 2nd Edition, Elsevier, 2023.

REFERENCES:

1. Chang Liu, Foundations of MEMS, 2nd Edition, Pearson Education, 2012.
2. Sergey Edward Lyshevski, Nano- and Micro-Electromechanical Systems: Fundamentals of Nano- and Microengineering, 2nd Edition, CRC Press, 2005.
3. Reza Ghodssi and Pinyen Lin (Editors), MEMS Materials and Processes Handbook, Springer, 2011.
4. Mohamed Gad-el-Hak (Editor), The MEMS Handbook, 2nd Edition, CRC Press, 2006.
5. Nadim Maluf and Kirt Williams, An Introduction to Microelectromechanical Systems Engineering, 2nd Edition, Artech House, 2004.
6. Vijay K. Varadan, K. J. Vinoy and K. A. Jose, RF MEMS and Their Applications, John Wiley & Sons, 2003.
7. Stephen D. Senturia, Microsystem Design, Springer, 2001.
8. Cornelius T. Leondes (Editor), MEMS/NEMS: Handbook Techniques and Applications, Springer, 2006.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	2	1	3	2	1
CO2	3	1	3	3	2
CO3	3	1	3	3	2
CO4	3	2	3	3	3
CO5	3	3	3	3	3
AVG	2.8	1.6	3	2.8	2.2

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


Chairman
Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

AE26015	CRYPTOGRAPHY AND NETWORK SECURITY	L	T	P	C
SDG: 16, 9		3	0	0	3

COURSE OBJECTIVES:

- Understand the fundamentals of information security and cryptography.
- Study symmetric and asymmetric cryptographic techniques.
- Understand authentication, digital signatures, and key management methods.
- Study network security, firewalls, VPNs, and web security technologies.
- Analyze wireless security challenges and secure communication techniques.

UNIT I INTRODUCTION ON SECURITY

9

Security Goals, Cryptographic attacks, Security services and mechanisms Techniques: Cryptography and Steganography, Traditional Symmetric-Key Ciphers: Substitution Ciphers and Transposition Ciphers, Mathematics for Cryptography.

UNIT II SYMMETRIC & ASYMMETRIC KEY ALGORITHMS

9

Introduction to Block Ciphers and Stream Ciphers, Data Encryption Standards (DES), Advanced Encryption Standard (AES), RC4, Principle of asymmetric key algorithms, RSA Cryptosystem.

UNIT III INTEGRITY, AUTHENTICATION AND KEY MANAGEMENT

9

Message Integrity, Hash functions: SHA 512, Whirlpool, Digital signatures: Digital signature standards. Authentication: Entity Authentication: Biometrics, Key management Techniques.

UNIT IV NETWORK SECURITY, FIREWALLS AND WEB SECURITY

9

Introduction on Firewalls, Types of Firewalls, IP Security, E-mail security: PGP- S/MIME, Web security: SSL-TLS, SET.

UNIT V WIRELESS NETWORK SECURITY

9

Security Attack issues specific to Wireless systems: Worm hole, Tunneling, DoS. Security for WLAN, Security for Broadband networks: Security challenges in 4G and 5G deployments, Introduction to side channel attacks and their counter measures.

ACTIVITIES:

1. Case Study: Enigma Machine and Cryptanalysis.
2. Case Study: Secure Banking Transactions using Public Key Cryptography.
3. Case Study: Digital Signature Applications in E-Governance.
4. Case Study: Enterprise Network Security Architecture
5. Review of GATE Questions.

COURSE OUTCOMES:

- CO1:** Explain information security concepts and cryptographic techniques.
- CO2:** Apply symmetric and asymmetric cryptographic algorithms for secure communication.
- CO3:** Evaluate authentication, digital signatures, and key management techniques.
- CO4:** Apply network and web security technologies to protect communication systems.
- CO5:** Analyze wireless security threats and develop suitable security solutions.

WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60% **TOTAL: 45 PERIODS**

TEXTBOOKS:

1. William Stallings, "Cryptography and Network Security: Principles and Practice", 8th Edition, Pearson Education, 2023.
2. Behrouz A. Forouzan and Debdeep Mukhopadhyay, "Cryptography and Network Security", 4th Edition, McGraw-Hill Education, 2015.

REFERENCES:

1. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security: Private Communication in a Public World", 3rd Edition, Pearson Education.
2. Atul Kahate, "Cryptography and Network Security", 4th Edition, McGraw-Hill Education.
3. Douglas R. Stinson and Maura Paterson, "Cryptography: Theory and Practice", 4th Edition, CRC Press.
4. Wenbo Mao, "Modern Cryptography: Theory and Practice", Pearson Education.
5. Bruce Schneier, "Applied Cryptography: Protocols, Algorithms and Source Code in C", Wiley India.

6. Nina Godbole and Sunit Belapure, "Cyber Security: Understanding Cyber Crimes, Computer Forensics and Legal Perspectives", Wiley India.
NIST Special Publications on AES, SHA, Digital Signatures, and Public Key Cryptography.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	1	1	3	1	1
CO2	3	1	3	2	2
CO3	3	2	3	2	2
CO4	3	2	3	3	2
CO5	3	2	3	3	3
AVG	2.6	1.6	3	2.2	2

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26016		NEUROMORPHIC COMPUTING				L	T	P	C
SDG: 9, 7						3	0	0	3
COURSE OBJECTIVES:									
- Understand the fundamentals of neuromorphic computing and brain-inspired systems. - Study spiking neural networks, neuron models, and learning techniques. - Design analog and mixed-signal circuits for neuromorphic systems. - Explore neuromorphic architectures, memory technologies, and emerging devices. - Develop neuromorphic solutions for AI, robotics, and sensor applications.									
UNIT I		BIOLOGICAL INSPIRATION AND NEURAL CODING							9
Biological neurons and synapses: structure and function, Spike generation and propagation (Hodgkin-Huxley, Integrate-and-Fire models), Neural coding: rate code, temporal code, population code, Synaptic plasticity: Hebbian learning, STDP (Spike-Timing-Dependent Plasticity), Functional models of neural computation.									
UNIT II		SPIKING NEURAL NETWORKS AND LEARNING ALGORITHMS							9
SNN architecture and neuron models (LIF, Izhikevich), Spike encoding and decoding techniques, Supervised and unsupervised learning: STDP, Reward-Modulated STDP, Reservoir computing and Liquid State Machines, SNN simulation frameworks: BRIAN2, NEST, PyNN.									
UNIT III		VLSI IMPLEMENTATION OF NEUROMORPHIC SYSTEMS							9
Analog and digital circuit models of neurons and synapses, Current-mode vs. voltage-mode designs, Subthreshold analog VLSI design for neuron circuits, Mixed-signal implementations and silicon neurons, Noise tolerance and power-efficiency in neuromorphic chips.									
UNIT IV		NEUROMORPHIC HARDWARE AND ARCHITECTURES							9
Architectures of Loihi (Intel), TrueNorth (IBM), SpiNNaker (Manchester), Memory-centric computing and synapse mapping, Memristor-based neuromorphic architectures, Emerging devices: Phase-change memory, Ferroelectric FETs, and STT-MRAM, Crossbar arrays and 3D integrated neuromorphic systems.									
UNIT V		APPLICATIONS AND TRENDS IN NEUROMORPHIC COMPUTING							9
Brain-computer interfaces (BCI), Edge computing using neuromorphic chips, Sensor fusion and neuromorphic perception (vision, auditory), Neuromorphic robotics and event-based control, Future directions: AI accelerators, quantum neuromorphic systems, ethical implications.									
ACTIVITIES:									
- Simulating Neural Spiking and Coding. - Build and Train a Simple Spiking Neural Network Using BRIAN2. - Design and Simulate a Subthreshold Analog Silicon Neuron. - Design a Neuromorphic Application for Edge Intelligence. - Review of GATE Questions.									
COURSE OUTCOMES:									

- CO1:** Explain neuron models and synaptic plasticity principles.
CO2: Analyze and implement spiking neural networks.
CO3: Design neuromorphic circuits for efficient neural computation.
CO4: Analyze neuromorphic hardware and emerging memory technologies.
CO5: Develop neuromorphic solutions for intelligent and edge AI applications.

TOTAL: 45 PERIODS

WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%

TEXTBOOKS:

1. Abdel-Hameed A. Badawy and Ahmed B. Abdallah, Neuromorphic Computing Principles and Organization, Springer, 2025.
2. Nan Zheng and Pinaki Mazumder, Learning in Energy-Efficient Neuromorphic Computing: Algorithm and Architecture Co-Design, John Wiley & Sons, 2020.
3. Nan Zheng and Pinaki Mazumder, Neuromorphic Computing: From Materials to Systems Architecture, CRC Press, 2022.

REFERENCES:

1. Yun Qu, Yi Zeng and Li Ma, Towards Neuromorphic Machine Intelligence, Elsevier, 2024.
2. Nikola K. Kasabov, Time-Space, Spiking Neural Networks and Brain-Inspired Artificial Intelligence, Springer, 2019.
3. Shih-Chii Liu, Tobi Delbruck, Giacomo Indiveri, Adrian Whatley and Rodney Douglas, Event-Based Neuromorphic Systems, John Wiley & Sons, 2015.
4. Steve Furber, SpiNNaker: A Spiking Neural Network Architecture, Now Publishers, 2020.
5. Qing Wu, Tielin Zhang and Haizhou Li, Neuromorphic Cognitive Systems: A Learning and Memory Centered Approach, Springer, 2017.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	1	1	3	1	1
CO2	3	1	3	2	3
CO3	3	1	3	3	3
CO4	2	1	3	3	2
CO5	3	2	3	3	3
AVG	2.4	1.2	3	2.4	2.4

1 – Low, 2 – Medium, 3 – High, '-' – no correlation


 Chairman
 Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

AE26017	AI HARDWARE ARCHITECTURES AND ACCELERATORS	L	T	P	C
SDG: 9, 4		3	0	0	3
COURSE OBJECTIVES: - Understand the fundamentals of AI, deep learning, neural networks, and AI hardware. - Study parallel computing architectures and AI accelerators. - Understand hardware techniques for accelerating deep neural networks. - Explore in-memory and near-memory computing for energy-efficient AI systems. - Design and evaluate AI hardware for edge and high-performance computing applications.					
UNIT I	INTRODUCTION TO DEEP LEARNING				9
Introduction to Deep Learning – Neural Network Models – Neural Network Classification – Neural Network Framework – Neural Network Comparison – Neural Network Layers – DNN Development Resources – Deep Learning Challenges – Key Metrics and Design Objectives.					
UNIT II	PARALLEL ARCHITECTURES				9
Central Processing Unit (CPU) – Graphics Processing Unit (GPU) – Deep Learning Accelerator (NVDLA) – Tensor Processing Unit (TPU) – Dataflow Accelerator – Streaming Graph Theory – Blaze Graph Streaming Processor – Graph core Intelligence Processing Unit.					
UNIT III	CONVOLUTION OPTIMIZATION				9
Deep Convolutional Neural Network Accelerator – Eyeriss Accelerator Architecture – Convolution Optimization Techniques – Data Reuse Strategies – Memory-Efficient CNN Processing – Hardware Mapping Techniques.					
UNIT IV	IN-MEMORY COMPUTATION AND NEAR-MEMORY ARCHITECTURE				9
Neurocube Architecture – Tetris Accelerator – NeuroStream Accelerator – DaDianNao Supercomputer – Cnvlutin Accelerator – In-Memory Computing – Near-Memory Processing Architectures.					
UNIT V	NETWORK SPARSITY AND 3D NEURAL PROCESSING				9
Network Sparsity – Energy Efficient Inference Engine – Cambricon-X Accelerator – SCNN Accelerator – SeeNet Accelerator – 3D Integrated Circuit Architecture – Power Distribution Network – 3D Network Bridge – Power Saving Techniques.					
ACTIVITIES: - Case Study on AI hardware requirements in autonomous vehicles and smart healthcare. - Case Study on Hardware acceleration in image recognition systems. - Case Study on Memory Bottleneck Problems in Deep Learning Accelerators. - Review of GATE Questions.					
COURSE OUTCOMES: CO1: Explain deep learning fundamentals and AI hardware requirements. CO2: Analyze parallel computing architectures for AI workloads. CO3: Design optimized CNN hardware accelerators. CO4: Analyze in-memory and near-memory AI computing architectures. CO5: Design power-efficient AI hardware for edge intelligence applications.					
TOTAL: 45 PERIODS					
WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%					
TEXTBOOKS: - Vivienne Sze, Yu-Hsin Chen, Tien-Ju Yang and Joel S. Emer, Efficient Processing of Deep Neural Networks: A Tutorial and Survey, Morgan & Claypool Publishers, 2020. - Vijay Janapa Reddi, Gu-Yeon Wei, David Brooks and Carole-Jean Wu, Machine Learning Systems: Design and Implementation of AI Accelerators, Springer, 2023. - Mohamed Elgendy, Deep Learning for Vision Systems: Architecture, Applications, and Hardware Acceleration, Manning Publications, 2020.					
REFERENCES: Norman P. Jouppi et al., In-Datcenter Performance Analysis of a Tensor Processing Unit, ACM/IEEE ISCA Proceedings, 2017.					

2. Yu-Hsin Chen, Joel Emer and Vivienne Sze, Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep CNNs, IEEE Journal of Solid-State Circuits, 2017.
 3. Tianshi Chen et al., DaDianNao: A Machine-Learning Supercomputer, IEEE/ACM MICRO, 2014.
 4. Sharan Narang et al., Accelerating Deep Learning Inference with Sparse Computation, IEEE Micro, 2018.
 5. Michael Gschwind, AI Hardware Architectures and Accelerators, Springer, 2021.
 6. John L. Hennessy and David A. Patterson, Computer Architecture: A Quantitative Approach, 6th Edition, Morgan Kaufmann, 2019.
- IEEE Transactions on Computers, IEEE Transactions on VLSI Systems, IEEE Transactions on Neural Networks and Learning Systems (Recent Research Articles).

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	1	1	3	1	1
CO2	2	1	3	2	2
CO3	3	1	3	3	3
CO4	3	1	3	3	3
CO5	3	2	3	3	3
AVG	2.4	1.2	3	2.4	2.4

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26018	IP CORE DESIGN AND PROTECTION	L	T	P	C
SDG: 9, 8		3	0	0	3

COURSE OBJECTIVES:

- Understand IP cores and their role in VLSI and SoC design.
- Study hardware IP types, reuse, verification, and integration techniques.
- Understand hardware IP security threats and protection methods.
- Explore watermarking, fingerprinting, and authentication techniques for IP protection.
- Study IP licensing, user rights management, and emerging security trends.

UNIT I	IP CORES DESIGN	9
---------------	------------------------	----------

Introduction: IP cores in a typical VLSI design flow, Classification of hardware IP, IP Modeling, IP Verification, IP Optimization, IP Protection, Gates as IP, Subsystems as IP, IP Components, Intellectual Property in Reuse-Based Design.

UNIT II	HARDWARE INTELLECTUAL PROPERTY PROTECTION	9
----------------	--	----------

Functional Obfuscation through State Transition Graph Modification, Extension of STG Modification for RTL Designs, Obfuscation through Control and Dataflow Graph (CDFG) Modification, Measure of Obfuscation Level, Design Flow, Implementation Results, Effect of Key Length.

UNIT III	CONSTRAINT-BASED IP PROTECTION	9
-----------------	---------------------------------------	----------

Solutions to SAT, FPGA Design of DES Benchmark, Graph Coloring and the CF IIR Filter Design, Constraint-Based Watermarking, Fingerprinting, Copy Detection, Challenges and the Generic Approach, Mathematical Foundations for the Constraint-Based Watermarking Techniques, Optimization-Intensive Watermarking Techniques.

UNIT IV	IP USER'S RIGHT PROTECTION	9
----------------	-----------------------------------	----------

Motivation and Challenges, Fingerprinting Objectives, Constraint-Based Fingerprinting Techniques.

UNIT V	IP AUTHENTICATION	9
---------------	--------------------------	----------

Introduction, Pattern Matching Based Techniques, Forensic Engineering Techniques, Public Detectable Watermarking Techniques.

ACTIVITIES:

1. Model and integrate a simple IP block (UART/FIFO) using Verilog/VHDL.
2. Simulate logic obfuscation techniques using HDL.
3. Design and evaluate a secure IP protection framework combining watermarking, fingerprinting, and authentication (Mini Project).
4. Review of GATE Questions.

COURSE OUTCOMES:**CO1:** Explain IP core concepts and SoC integration methodologies.**CO2:** Analyze hardware IP protection and security techniques.**CO3:** Apply watermarking, fingerprinting, and authentication methods.**CO4:** Evaluate hardware IP attacks and countermeasures.**CO5:** Analyze IP rights management and secure commercialization strategies.**TOTAL: 45 PERIODS****WEIGHTAGE:** Continuous Assessment: 40%, End Semester Examinations: 60%**ASSESSMENT METHODOLOGY:** Quiz (10%), Assignments/Activities (40%), Flipped class (10%), Internal Examinations (40%)**TEXTBOOKS:**

1. Andrew B. Kahng, Igor L. Markov, Jens Lienig, Jin Hu and Valeria Bertacco, VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer, 2nd Edition, 2022.
2. Swarup Bhunia and Mark Tehranipoor, Hardware Security: A Hands-on Learning Approach, Morgan Kaufmann, 2018.
3. Rolf Drechsler and Jörg Becker, Advanced Hardware Design for Error Correcting Codes and Security Applications, Springer, 2015.

REFERENCES:

1. Rajat Subhra Chakraborty and Swarup Bhunia, Hardware Protection and Authentication through Embedded Watermarking, Springer, 2010.
2. Yier Jin and Swarup Bhunia, Hardware Protection through Obfuscation and Logic Locking, Springer, 2018.
3. Farinaz Koushanfar and Miodrag Potkonjak, Intellectual Property Protection in VLSI Designs: Theory and Practice, IEEE Design & Test of Computers, Vol.19, No.4.
4. Mark Tehranipoor and Cliff Wang, Counterfeit Integrated Circuits: Detection and Avoidance, Springer, 2015.
5. Miodrag Potkonjak, Techniques for Intellectual Property Protection of Integrated Circuits, IEEE Signal Processing Magazine, Vol.24, No.3.
6. Jens Lienig and Juergen Scheible, Fundamentals of Electronic Systems Design, Springer, 2020.
7. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Recent articles on Hardware Security, IP Protection, Watermarking and Logic Locking.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	1	1	3	2	2
CO2	3	1	3	2	2
CO3	3	2	3	3	2
CO4	3	2	3	3	3
CO5	2	3	3	2	2
AVG	2.4	2.2	3	2.4	2.2

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


 Chairman
 Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059

AE26019	SPINTRONICS AND QUANTUM COMPUTING			L	T	P	C
SDG: 9, 7				3	0	0	3
COURSE OBJECTIVES:							
- Understand the fundamentals of spintronics and spin-dependent transport. - Study spintronic devices, magnetic memories, and emerging architectures. - Understand qubits, quantum gates, and quantum algorithms. - Study quantum error correction and fault-tolerant computing techniques. - Explore quantum computing hardware and its integration with spintronics.							
UNIT I	FUNDAMENTALS OF SPINTRONICS						9
Electron spin, spin angular momentum, Pauli exclusion principle, Ferromagnetism, magnetic domains, exchange interaction, Spin injection and detection, Giant magnetoresistance (GMR), tunneling magnetoresistance (TMR), Spin polarization and spin coherence.							
UNIT II	SPIN-BASED DEVICES AND ARCHITECTURES						9
Spin valves, magnetic tunnel junctions (MTJs), Spin Field Effect Transistors (Spin FETs), Domain wall logic and racetrack memory, Spin torque oscillators, STT-MRAM, SOT devices, Fabrication challenges and materials for spintronic devices.							
UNIT III	INTRODUCTION TO QUANTUM COMPUTING						9
Qubits: physical realization and quantum state representation, Quantum gates and circuits: single- and multi-qubit operations, Quantum superposition and entanglement, No-cloning theorem and quantum teleportation, Reversible logic and quantum circuit metrics.							
UNIT IV	QUANTUM ALGORITHMS AND ERROR CORRECTION						9
Quantum parallelism and the Deutsch-Jozsa algorithm, Grover's algorithm and search speedup, Shor's algorithm for integer factorization, Quantum error correction codes (bit flip, phase flip, Shor code), Basics of quantum fault tolerance.							
UNIT V	HARDWARE REALIZATIONS AND SPIN-QUBIT INTEGRATION						9
Physical qubit implementations: superconducting, trapped ion, spin qubits; Semiconductor spin qubits: GaAs and Si-based platforms, NV centers in diamond and quantum dots, Integration of spintronics with quantum computing hardware, Cryogenic control and coherence time limitations.							
ACTIVITIES:							
- Simulate GMR and TMR effects using any Numerical computing and simulation tool. - Model and compare the characteristics of Spin FET, MTJ, and STT-MRAM devices using any device simulation tool. - Design a conceptual spin-based quantum computing architecture (Mini Project) - Review of GATE Questions.							
COURSE OUTCOMES:							
CO1: Explain the fundamentals of spintronics and spin-dependent phenomena.							
CO2: Analyze spintronic devices, memories, and architectures.							
CO3: Apply quantum computing concepts and design basic quantum circuits.							
CO4: Implement quantum algorithms and error correction techniques.							
CO5: Evaluate quantum hardware and spin-based quantum technologies.							
TOTAL: 45 PERIODS							
WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%							
TEXTBOOKS:							
- Supriyo Bandyopadhyay and Marc Cahay, Introduction to Spintronics, 2nd Edition, CRC Press, 2016. - Michael A. Nielsen and Isaac L. Chuang, Quantum Computation and Quantum Information, 10th Anniversary Edition, Cambridge University Press, 2010/2012. - Chris Bernhardt, Quantum Computing for Everyone, MIT Press, 2019.							
REFERENCES:							
- Jack D. Hidary, Quantum Computing: An Applied Approach, 2nd Edition, Springer, 2021. - Eleanor G. Rieffel and Wolfgang H. Polak, Quantum Computing: A Gentle Introduction, MIT Press, 2011. - David McMahon, Quantum Computing Explained, John Wiley & Sons, 2008.							

4. Supriyo Bandyopadhyay, Magnetic Straintronics, Springer, 2024.
5. Supriyo Bandyopadhyay, Nanomagnets as Dynamical Systems: Primer and Applications, Springer, 2024.
- Hamed N. Nazemi and Massoud Pedram, Hardware for Quantum Computing, Springer, 2024.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	1	-	3	2	2
CO2	2	1	3	3	2
CO3	2	1	3	2	2
CO4	3	2	3	2	3
CO5	3	2	3	3	3
AVG	2.2	1.2	3	2.4	2.4

1 - Low, 2 - Medium, 3 - High, '-' - no correlation

AE26020	ROBOTICS AND INTELLIGENT SYSTEMS				L	T	P	C
SDG: 9, 11					3	0	0	3

COURSE OBJECTIVES:

- Understand the fundamentals of robotics and industrial automation.
- Study robot grippers and sensors used in robotic systems.
- Understand robot drives, actuators, and control techniques.
- Apply machine vision and programming techniques for robotic applications.
- Explore intelligent robotics and modern automation technologies.

UNIT I	INTRODUCTION TO ROBOTICS AND AUTOMATION	9
---------------	--	----------

Introduction to Robotics – Laws of Robotics – Robot anatomy – Degrees of Freedom (DOF) – Classification of robots – Robot performance parameters: Resolution, accuracy, repeatability, dexterity and compliance – Fundamentals of automation – Need and applications of automation – Basic elements of automated systems – Levels of automation – Industrial applications of robotics and automation.

UNIT II	ROBOT GRIPPERS AND SENSORS	9
----------------	-----------------------------------	----------

Types of robot grippers – Mechanical, magnetic, vacuum and adaptive grippers – Gripper selection and design considerations – Gripping force analysis – Fundamentals of robotic sensors – Sensor characteristics and selection – Position, proximity, force, torque and tactile sensors – Applications of sensors in robotic systems.

UNIT III	DRIVES AND CONTROL SYSTEMS	9
-----------------	-----------------------------------	----------

Electric, hydraulic and pneumatic drives – Robot actuators – Selection of drives and actuators – Mechanical transmission systems – Fundamentals of robot control – Open-loop and closed-loop control systems – Position, velocity and force control – Sensors and actuators in robot control – Industrial robot controllers.

UNIT IV	MACHINE VISION AND ROBOT PROGRAMMING	9
----------------	---	----------

Fundamentals of machine vision – Components of a machine vision system – Image acquisition – Image preprocessing – Feature extraction – Object detection and recognition – Applications of machine vision in robotics – Methods of robot programming – Lead-through and offline programming – Motion commands – Motion interpolation – Branching, delay and subroutine operations.

UNIT V	INTELLIGENT ROBOTICS AND AUTOMATION	9
---------------	--	----------

Industrial applications of robots – Robots in manufacturing, assembly, material handling and inspection – Artificial Intelligence in robotics – Machine learning for robotic applications – Artificial Neural Networks in automation – Fuzzy logic-based robot control – Collaborative robots – Autonomous robots – Safety in robotic systems – Emerging trends in robotics and automation.

ACTIVITIES:

1. Model and simulate a basic robotic manipulator and analyze its Degrees of Freedom (DOF), workspace, accuracy, and repeatability using any robotics simulation tool.
2. Design and simulate a robotic gripper and interface position, proximity, force, or tactile sensors for object detection and handling.
3. Simulate the position and speed control of DC, servo, or stepper motors using suitable control techniques.

4. Implement object detection and recognition using any image-processing tool and develop a basic robot program for pick-and-place operation.
5. Develop a simple AI-based autonomous or collaborative robotic application using any robotics simulation platform.
6. Review of GATE Questions.

45 PERIODS

COURSE OUTCOMES:

- CO1:** Explain the fundamentals of robotics and automation.
CO2: Analyze robot grippers and select suitable sensors.
CO3: Select suitable drives and control techniques for robotic systems.
CO4: Apply machine vision and programming techniques in robotics.
CO5: Develop intelligent robotic solutions for industrial automation.

WEIGHTAGE: Continuous Assessment: 40%, End Semester Examinations: 60%

TEXTBOOKS:

1. Mikell P. Groover, Automation, Production Systems, and Computer-Integrated Manufacturing, 5th Edition, Pearson, 2020.
2. Saeed B. Niku, Introduction to Robotics: Analysis, Control, Applications, 3rd Edition, John Wiley & Sons, 2020.
3. John J. Craig, Introduction to Robotics: Mechanics and Control, 4th Edition, Pearson, 2018.

REFERENCES:

1. Bruno Siciliano, Lorenzo Sciavicco, Luigi Villani and Giuseppe Oriolo, Robotics: Modelling, Planning and Control, 2nd Edition, Springer, 2022.
2. Kevin M. Lynch and Frank C. Park, Modern Robotics: Mechanics, Planning, and Control, Cambridge University Press, 2017.
3. Peter Corke, Robotics, Vision and Control: Fundamental Algorithms in MATLAB, 3rd Edition, Springer, 2023.
4. Mark W. Spong, Seth Hutchinson and M. Vidyasagar, Robot Modeling and Control, 2nd Edition, John Wiley & Sons, 2020.
5. Shimon Y. Nof (Editor), Springer Handbook of Automation, 2nd Edition, Springer, 2023.
6. Bruno Siciliano and Oussama Khatib (Editors), Springer Handbook of Robotics, 2nd Edition, Springer, 2016.

CO's-PO's & PSO's MAPPING

CO	PO1	PO2	PO3	PSO1	PSO2
CO1	1	-	2	2	1
CO2	2	-	3	3	2
CO3	3	1	3	3	2
CO4	3	1	3	3	3
CO5	3	2	3	3	3
AVG	2.4	0.8	2.8	2.8	2.2

1 - Low, 2 - Medium, 3 - High, '-' - no correlation


 Chairman
 Board of Studies
 Department of Electronics and Communication Engineering
 Kingston Engineering College
 Vellore - 632 059