DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Innovations in teaching learning Process

Subject Code/Subject Name: EC 6304 – Electronic Circuits I

Semester/Branch: III/ECE

Academic Year: 2015-2016 (ODD)

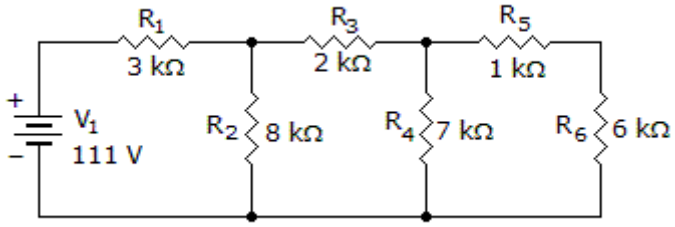
Quiz/Puzzle

1. What theorem replaces a complex network with an equivalent circuit containing a source voltage and a series resistance?

   A. Multinetwork
   B. Norton
   C. Thevenin
   D. Superposition

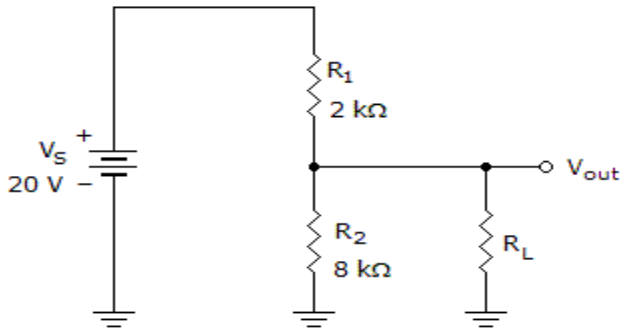
Ans: C

2. What is the power dissipated by R2, R4, and R6?



A.P2 = 417 mW, P4 = 193 mW, P6 = 166 mW
B.P2 = 407 mW, P4 = 183 mW, P6 = 156 mW
C.P2 = 397 mW, P4 = 173 mW, P6 = 146 mW
D.P2 = 387 mW, P4 = 163 mW, P6 = 136 mW
Ans: A

3.



If the load in the given circuit is 120 k , what is the loaded output voltage?

A 4.21 V
.
B.15.79 V
C.16 V
D 19.67 V
.
Ans: B

4.
In a series–parallel circuit, individual component power dissipations are calculated using:

A. individual component parameters
B. a percent of the voltage division ratio squared
C. total current squared multiplied by the resistor values
D. a percent of the total power depending on resistor ratios

Ans: A

5. The current flowing through an unloaded voltage divider is called the:

A. resistor current
B. load current
C. bleeder current
D. voltage current

Ans: C

6. When a Wheatstone bridge is in a balanced condition, the center voltmeter in the bridge will read:

A. twice the source voltage
B. the same as the source voltage
C. zero volts
D. half the source voltage

Ans: C

7. When a load is connected to a voltage divider, the total resistance of the circuit will:

7.

A. Decrease
B. Double
C. Increase
D. remain the same

Ans: A

8. With 21 V applied, if R_1 = 5 ohms, R_2 = 35 ohms, and R_3 = 14 ohms, what is the current of R_2 if R_1 is series connected with parallel circuit R_2 and R_3?

A. 200 mA
B. 800 mA
C. 600 mA
D. 400 mA

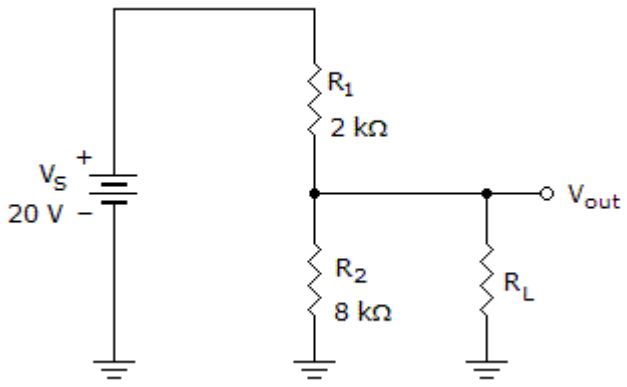
Ans: D

9. What is the total resistance of a circuit when R_1 (7 kΩ) is in series with a parallel combination of R_2 (20 kΩ), R_3 (36 kΩ), and R_4 (45 kΩ)?

A. 4 kΩ
B. 17 kΩ
C. 41 kΩ
D. 108 kΩ

Ans: B

10.



If the load in the given circuit is 80 kΩ , what is the ***bleeder current***?

A. 196 µA

.
B.1.96 mA
C.2 mA
D 2.16 mA
.

Ans: B

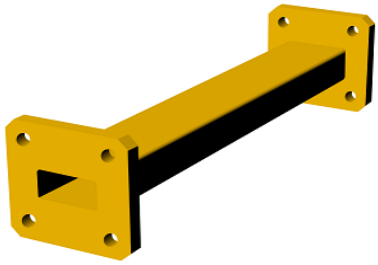
Subject Code/Subject Name: EC 6503 - Transmission Lines and Waveguides

Semester/Branch: V/ECE

Academic Year: 2015-2016 (ODD)

Quiz/Puzzle

1. Identify the below figure with the clue given



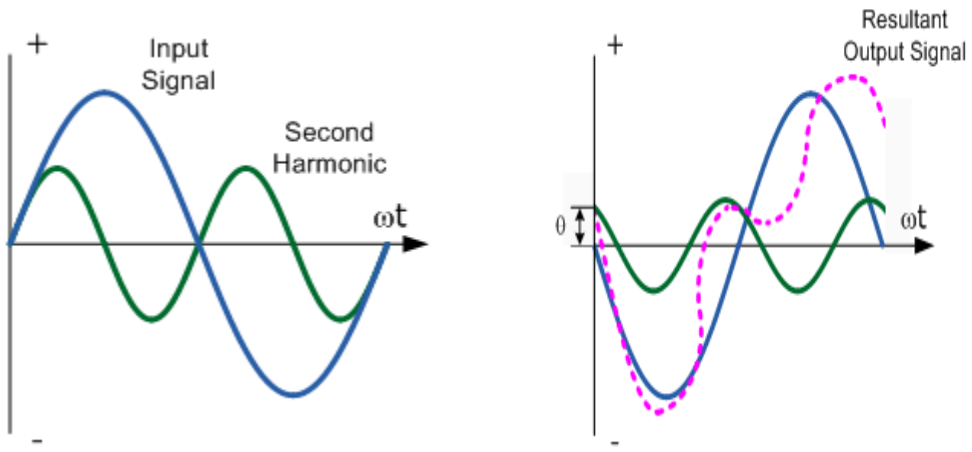
Energy Transmission

The transfer of energy from one place to another place takes place through …….

Ans : waveguide

2. What do you infer from the below diagram??? Can you guess the process????

DELAY



All the frequencies applied to the transmission line will not travel uniformly, some of them may be delayed more than others. The phenomenon is known as
…….

Ans : Phase Distortion

3.

lumped loading

By the above process which factor of the transmission lines will be increased

a) CAPACITANCE

b) RESISTANCE

c) INDUCTANCE

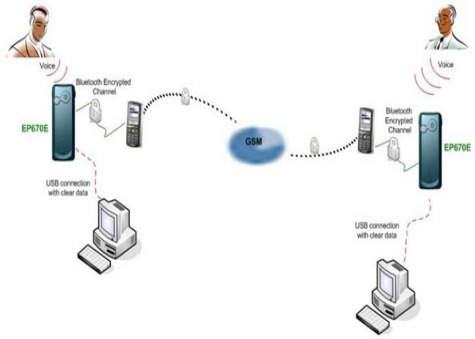
d) ALL THE ABOVE

The …….. of a transmission line can be increased by the introduction of loading coils at uniform intervals is called as lumped loading.

Ans : Inductance

4. Delay distottion is very important in which of the following Transmission

a)



b)

The distortion which is less importance to voice transmission and very serious in case of video transmission , the distortion is called as …… distortion.

Ans : Delay

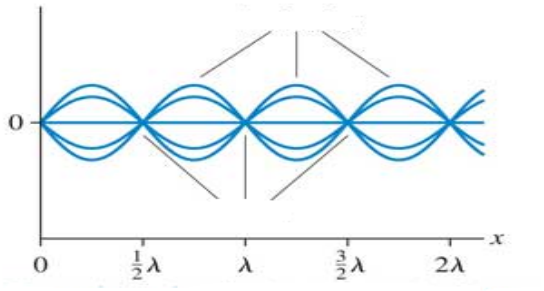
5.

INCIDENT WAVE+ REFLECTED WAVES

The combination of incident waves and reflected waves is called as ……

Ans : standing wave

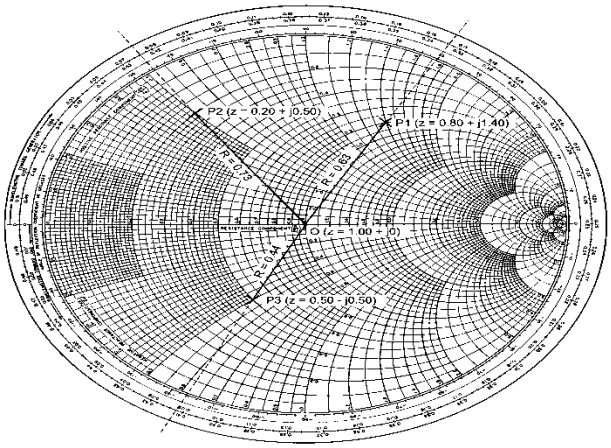
6. Find out what does the arrows point to???



…….. or loops are points of maximum voltage or current in standing waves.

Ans : Antinodes

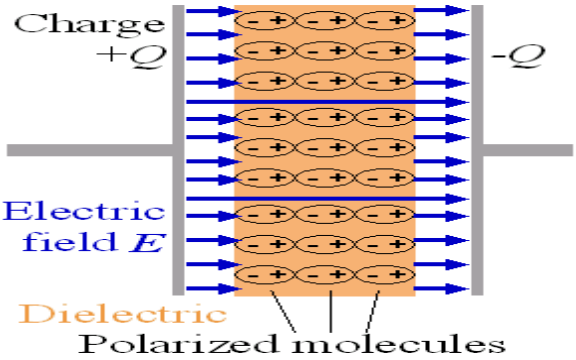
7. Guess the name of the below chart



Ans : Smith chart

8. The transformation utilized for formulating the smith chart is called as …… transformation.
   Ans : Molius.
9.

EM WAVES



The electromagnetic waves that are guided along or over conducting or dielectric surfaces are called …….waves.
Ans : guided

10. ……. electric waves are waves in which the electric field strength E is entirely transverse.
    Ans : transverse

11. At cut-off frequency the wave impedence becomes ……. For TE waves.
    Ans : infinity

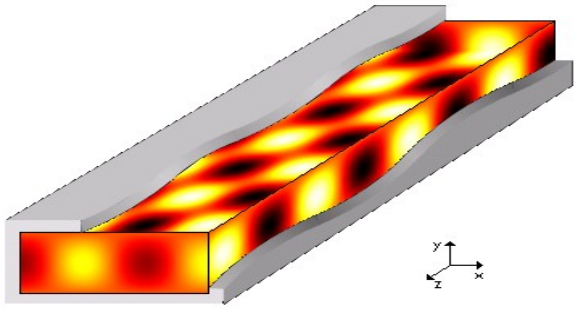
12. The wave impedence for TEM wave is ……

    Ans : intrinsic impedence

13. …….. …… is defined as the ratio of electric field intensity to the magnetic field intensity.

    Ans : Wave impedence

14 .



A hollow conducting metallic tube of uniform cross section is used for propagating ……. Waves.

Ans : Electromagnetic

15 . At cut-off frequency the wave impedence for TM wave becomes ……..

Ans : zero

16. The lowest order mode is called as …… mode.

Ans : Dominant

17. The waveguide which offers the maximum attenuation is ……

Ans :coaxial

18 . A circular waveguide will behave like a ……. …….. filter.

Ans : high pass

19. Circular waveguides are used as …… and phase shifters.

Ans : Attenuators

20. A ……. Cavity resonator is a circular waveguide with two ends closed by a metal.

Ans : Circular

Subject Code/Subject Name: EC 6601 – VLSI Design

Semester/Branch: VI/ECE

Academic Year: 2015-2016 (EVEN)

Group Discussion

The Future of Very Large-Scale Integration (VLSI) Technology

A group of seven members formed to discuss about the Future of VLSI Technology and the students were actively participated in it. The crisp of the discussion is presented over here.

Student 1: The historical growth of IC computing power has profoundly changed the way we create, process, communicate, and store information. The engine of this phenomenal growth is the ability to shrink transistor dimensions every few years. This trend, known as Moore's law, has continued for the past 50 years.

Student 2: The predicted demise of Moore's law has been repeatedly proven wrong thanks to technological breakthroughs (e.g., optical resolution enhancement techniques, high-k metal gates, multi-gate transistors, fully depleted ultra-thin body technology, and 3-D wafer stacking).

Student 3: it is projected that in one or two decades, transistor dimensions will reach a point where it will become uneconomical to shrink them any further, which will eventually result in the end of the CMOS scaling roadmap.

Student 1: Steep transistors: The ability to scale a transistor's supply voltage is determined by the minimum voltage required to switch the device between an on- and an off-state. The sub-threshold slope (SS) is the measure used to indicate this property. For instance, a smaller SS means the transistor can be turned on using a smaller supply voltage while meeting the same off current. For MOSFETs, the SS has to be greater than $\ln(10) \times kT/q$ where k is the Boltzmann constant, T is the absolute temperature, and q is the electron charge. This fundamental constraint arises from the thermionic nature of the MOSFET conduction mechanism and leads to a fundamental power/performance tradeoff, which could be overcome if SS values significantly lower than the theoretical 60-mV/decade limit could be achieved. Many device types have been proposed that could produce steep SS values,

including tunneling field-effect transistors (TFETs), nanoelectromechanical system (NEMS) devices, ferroelectric-gate FETs, and impact ionization MOSFETs.

Student 4: Several recent papers have reported experimental observation of SS values in TFETs as low as 40 mV/decade at room temperature. These so-called “steep” devices’ main limitations are their low mobility, asymmetric drive current, bias dependent SS, and larger statistical variations in comparison to traditional MOSFETs.

Student 2: Spin devices: Spintronics is a technology that utilizes nano magnets’ spin direction as the state variable. Spintronics has unique properties over CMOS, including nonvolatility, lower device count, and the potential for non-Boolean computing architectures. Spintronics devices’ nonvolatility enables instant processor wake-up and power-down that could dramatically reduce the static power consumption. Furthermore, it can enable novel processor-in-memory or logic-in-memory architectures that are not possible with silicon technology. Although in its infancy, research in spintronics has been gaining momentum over the past decade, as these devices could potentially overcome the power bottleneck of CMOS scaling by offering a completely new computing paradigm.

Student 5: In recent years, progress has been made toward demonstration of various post-CMOS spintronic devices including all-spin logic, spin wave devices, domain wall magnets for logic applications, and spin transfer torque magnetoresistive RAM (STT-MRAM) and spin-Hall torque (SHT) MRAM for memory applications. However, for spintronics technology to become a viable post-CMOS device platform, researchers must find ways to eliminate the transistors required to drive the clock and power supply signals. Otherwise, the performance will always be limited by CMOS technology. Other remaining challenges for spintronics devices include their relatively high active power, short interconnect distance, and complex fabrication process.

Student 6: Flexible electronics: Distributed large area (cm2-to-m2) electronic systems based on flexible thin-film-transistor (TFT) technology are drawing much attention due to unique properties such as mechanical conformability, low temperature processability, large area coverage, and low fabrication costs. Various forms of flexible TFTs can either enable applications that were not achievable using traditional silicon based technology, or surpass them in terms of cost per area. Flexible electronics cannot match the performance of silicon-based ICs due to the low carrier mobility. Instead, this technology is meant to complement them by enabling distributed sensor systems over a large area with moderate performance (less than 1 MHz).

Student 7: Development of inkjet or roll-to-roll printing techniques for flexible TFTs is underway for low-cost manufacturing, making product-level implementations feasible. Despite these encouraging new developments, the low mobility and high sensitivity to processing parameters present major fabrication challenges for realizing flexible electronic systems.

Student 7:Conclusion

CMOS scaling is coming to an end, but no single technology has emerged as a clear successor to silicon. The urgent need for post-CMOS alternatives will continue to drive high-risk, high-payoff research on novel device technologies. Replicating silicon’s success might

sound like a pipe dream. But with the world’s best and brightest minds at work, we have reasons to be optimistic.